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AMI® 6800 Microprocessors

S6800 Microprocessors

The following Advance Product Descriptions cover AMI's full family of 6800 Microprocessor circuits. For specific information on applications, product availability and ordering information, please contact the nearest AMI sales office listed in the back of this brochure. Or call David Gellatly, Manager, Microprocessor Product Marketing, at (408) 246-0330.

Revised October 1975

S6800 Microprocessing Family Selection Guide

Part No.	Description	Input/ Output	Power Supply (V)	Process	Package	See Page
S6800	Processor (8-bit)	TTL	+5V	N-SiGate	40 PIN	18
S6810	RAM (128 x 8)	TTL	+5V	N-SiGate	24 PIN	36
S6830	ROM (1024 x 8)	TTL	+5V	N-SiGate	24 PIN	40
S6820	Peripheral Interface Adaptor	TTL	+5V	N-SiGate	40 PIN	44
S6850	Asynchronous Communications Interface	TTL	+5V	N-SiGate	24 PIN	56
S6860	Digital Modem	TTL	+5V	N-SiGate	24 PIN	66
S2350	Synchronous Receiver/Transmitter	TTL	+5V	N-SiGate	40 PIN	84
S6834	Eraseable and Electrically Reprogrammable ROM (512 x 8)	TTL	+5, –12	P-SiGate	24 PIN	93
S4021	RAM (4096 x 1)	TTL	±5V, +12V	N-SiGate	22 PIN	99

S6800 Support Literature

Assembly Language Programming Manual ($15)
Hardware Reference Manual ($15)
6800 Simulator Manual
NCSS Timesharing Users Guide
Guide to Standard MOS Products

Future Products

S6831 Read Only Memory, 2048 x 8 – a mask programmable MOS memory, organized to be compatible with the S6800 MPU. The data, address, and control lines match those of the MPU, all signal levels are TTL compatible and it operates on a +5V power supply.

S6800 Microprocessing Family

S6800 Microprocessor (MPU) – an 8-bit parallel processor, with the ability to address up to 65K bytes of memory, and execute instructions in 2 microseconds. It is manufactured using N-channel MOS technology and operates on a single +5V power supply. All inputs and outputs are TTL compatible. The MPU has six internal registers, four types of vectored interrupts and 72 basic instructions. The basic instructions can be used in different addressing modes to save instruction execution time and memory space.

S6810 Static Read/Write Memory, 128 x 8 – an N-channel MOS memory designed and organized to be compatible with the S6800 MPU. Its data, address and control line organization and functions match those of the MPU, all signal levels are TTL compatible and no clocks or refreshing are needed. There are two versions of this memory: S6810 with 1.0 μsec maximum access time, and S6810-1 with 575 nsec. maximum access time.

S6830 Read Only Memory, 1024 x 8 – an N-channel MOS mask programmable read only memory that is used for storing the S6800 MPU operating programs. Like the S6810 RAM, this ROM has data, address, and control line organization that is compatible with that of the MPU. Its signal levels are TTL compatible and it can be accessed in a maximum of 575 nsec.

S6820 Peripheral Interface Adapter (PIA) – a general purpose programmable interface circuit that provides the means for most any kind of peripheral device or circuit to communicate with the S6800 MPU. The PIA has two 8-bit input/output ports for communicating with the peripherals and the MPU can program either port to send or receive data. Each port has two control lines associated with it. These also can be programmed by the MPU to handle interrupt and handshake routines with the peripherals.

S6850 Asynchronous Communication Interface Adapter (ACIA) – a general purpose communications interface that allows an asynchronous serial communications device to transmit data to and receive data from a S6800 microcomputer system. The ACIA can be programmed for handling different word lengths at various data rates; it also has parity generation and checking capability. For interfacing with the S6860 modem, the ACIA provides three status and command lines.

S6860 Modem – A 0-600 bps digital modem providing the necessary modulation, demodulation and supervisory controls to implement a serial data communications link over a voice grade channel. The modem is fully compatible with the S6800 microcomputer system, interfaces directly with the S6850 ACIA, and can be used in a wide variety of stand-alone modems, data communication terminals, I/O interfaces, and other data handling systems. N-channel silicon gate technology permits the modem to operate on a single +5V power supply and its inputs and outputs are TTL.

S6800 SYSTEM COMPATIBLE COMPONENTS

S2350 Universal Synchronous Receiver/Transmitter (USRT) – a general purpose communications interface that allows a high speed synchronous communications device to transmit data to and receive data from a S6800 microcomputer system. It connects to the peripheral device via separate serial transmit and receive lines and to the S6800 system data and address bus through a S6820 PIA.

The USRT has separate internal receiver and transmitter sections, which can be clocked by two separate clocks. It has the capability to handle different word lengths, generate and check parity and other conditions, detect sync during receive, and send a fill character during transmit operation.

S4021 Random Access Memory, 4096 x 1 – an N-channel Si-gate dynamic RAM for large volume low cost read/write storage. This memory has TTL compatible inputs and outputs, that can be easily interfaced to the S6800 system bus, access times as low as 200 nsec, and it operates on a single clock/chip-enable signal.

S6800 Microcomputer Systems

LSI FAMILY

The AMI S6800 Microprocessing Family is a series of matched MOS large scale integrated circuits for building microcomputer systems. In the same way as individual logic elements and subsystem functions in SSI and MSI* families are building blocks for random logic circuits, so the AMI S6800 LSI circuits are a family of building blocks for microcomputer systems.

The LSI family, however, is also very different from SSI/MSI. With LSI, the hardware designer can deal with whole subsystems, instead of individual logic elements: his design task is much simpler and faster; the functional complexity of the final system can be greatly increased, while its physical size is reduced.

Another difference relates to applications. Because a microcomputer system can be programmed, whereas a random logic circuit generally cannot, the LSI family is primarily used for different applications than those of SSI/MSI. It certainly overlaps the SSI/MSI applications, because LSI microcomputers can be used advantageously in direct replacement of random logic circuits (they can be programmed to perform the same functions), but the most important applications of microcomputers are in the areas where random logic circuits cease to be practical. A microcomputer can typically perform tasks that would require extremely complex and space consuming random logic circuits, because programming gives the microcomputer a whole order of added capability.

AMI S6800

The AMI S6800 Microprocessing Family hardware includes a microprocessor, ROM and RAM memories, and data input/output circuits. These components may be assembled in a building block manner into a very simple microcomputer system, or into any of progressively more complex systems, which can be used in many general or special purpose applications. The important feature of the S6800 family is that within any system all components are directly compatible in signal functions, circuit performance characteristics, and logic levels. All operate on a single +5V power supply.

**SSI and MSI – small scale and medium scale integration.*

It remains to the user to integrate the microcomputer into his own large system and to program it for a specific task. The task may be either simple or complex and either general in purpose or highly specialized for one application.

To facilitate system design and programming, AMI will provide a comprehensive set of reference documents, design and programming aids, a program library, and other applications support. For example, AMI will make available a comprehensive hardware and software reference manual, a S6800 program assembler, and a simulator. Such design and programming support is a continuing and expanding effort at AMI.

BASIC S6800 MICROCOMPUTER SYSTEM

A basic system built with the S6800 components is shown in Figure 1. In this system the S6800 Microprocessor (MPU) is supported by over 1K bytes of memory and controls one input/output interface circuit. The 1024-byte ROM is used to store the operating program, the 128-byte RAM provides working storage for the MPU, and the Peripheral Interface Adapter (PIA) provides two independently programmable 8-bit input/output ports for communicating with two peripheral devices.

The S6800 system is bus oriented. Eight lines form the data bus and 16 more lines make up the address bus. The MPU controls the bus and all other devices – the memories and the PIA – attach to the busses and wait for instructions from the MPU to supply or receive data. In the basic system, Figure 1, the MPU uses address lines A2, A13, and A14 to select one of the three devices on the bus and the Read/Write and Valid Memory Address lines to instruct the devices to receive or send data to the MPU. When communicating with the PIA, address lines A0 and A1 are used to select among the two peripheral devices A and B; the CA1, CA2, CB1, and CB2 lines can be used to send out control signals to the peripherals, or receive interrupts.

The basic system is a complete microcomputer, which can be used for a large variety of applications. It is simple but versatile, because it can be easily reprogrammed by changing the ROM. The user must provide only the two-phase clock signal source, a power-up/restart circuit, and a single +5V power supply to complete the hardware.

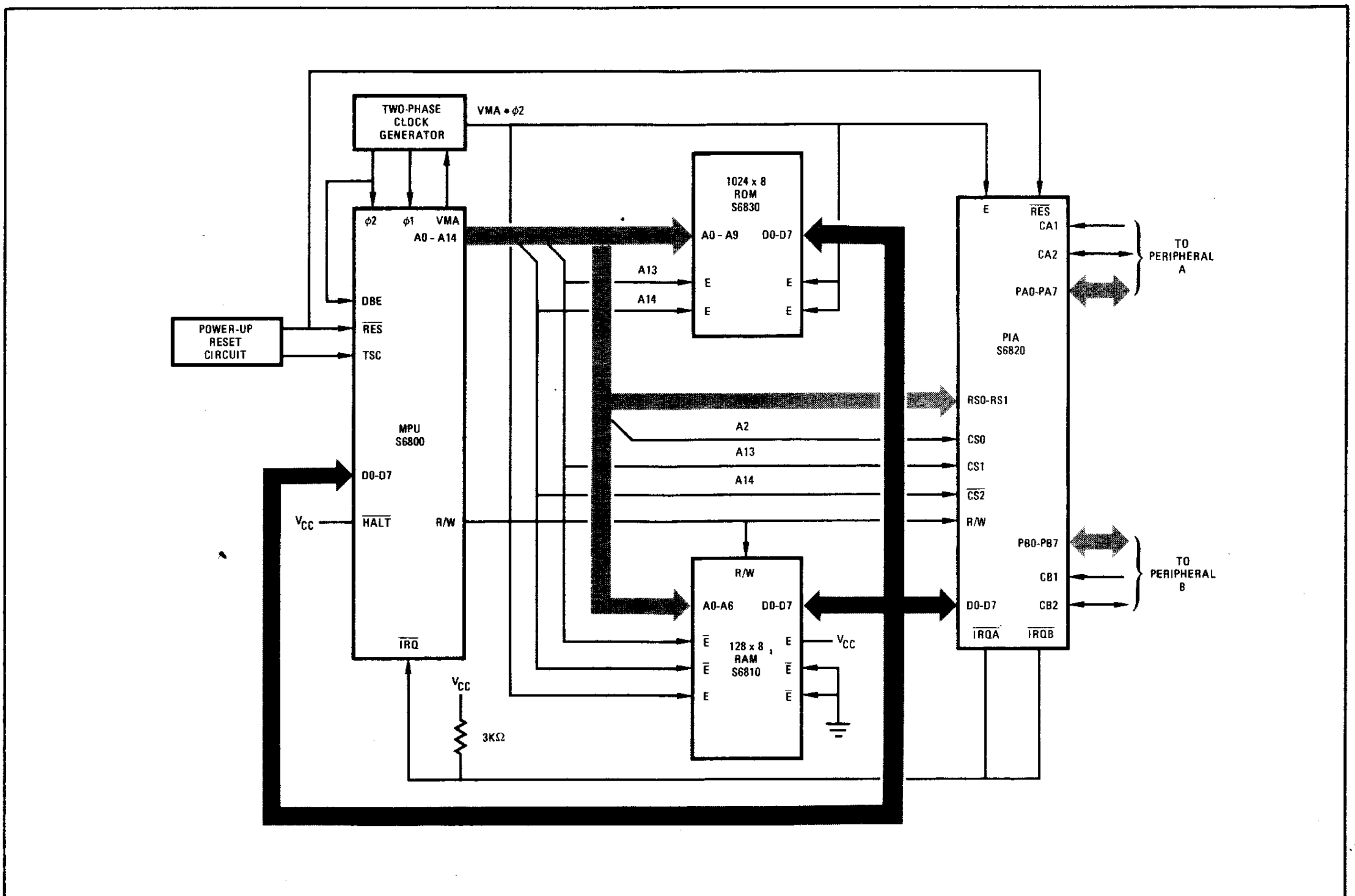
EXPANDING THE S6800 SYSTEM

The basic system can be altered or expanded in many different ways. For example, the S6850 Asynchronous Communication Interface Adapter (ACIA) can be substituted for the PIA, to enable the microcomputer to interface with a telecommunications modem. Or, additional memory can be added – either RAM or ROM – to expand the processing capability of the MPU. In general, the system can be expanded in a modular manner, by adding onto the bus as many as ten devices out of the S6800 family. These can be any combination of memory or input/output interface circuits. In this manner a system of nearly any complexity and configuration can be assembled. (Systems with more than ten devices on the bus require the addition of address and data bus buffers to operate at full speed.)

By building your microcomputer from the S6800 family of devices, you take advantage of the compatibility of the devices. They all conform to the bus discipline, all are compatible in load levels, and the entire system runs on a common system clock. In effect, you eliminate most all circuit design, save for the simple clock and power-up/restart circuits. Because you are dealing with only a small number of integrated circuits, circuit layout is simple and the entire microcomputer can be located on a single circuit card.

In some special purpose applications you may need to attach your own interface devices to the bus. As a result, more circuit design will be required, but you will find the S6800 MPU easy to work with. It has features that allow it to be used in many different systems. For example, by using the Halt, Three State Control, and Data Bus Enable lines you can easily design a direct memory access system, in which either the MPU or a peripheral device can read or write into the RAM and utilize the bus on a priority basis. You can also design a multiprocessor system, in which several MPUs can be attached to the same bus and share processing assignments, as well as memory space.

FIGURE 1 BASIC S6800 MICROCOMPUTER SYSTEM



S6800 INPUT/OUTPUT

One of the most important advantages that any S6800 system has to offer is its input/output versatility. In any computer system, large or small, the CPU internal functions are determined by the architecture of the computer and the user usually has little opportunity or need to alter them. On the other hand, the I/O configuration is almost always determined by the user and subject to change as peripherals are added or other system alterations are introduced. The I/O configuration is important to the user because it can affect the efficiency of the CPU itself, it determines the ease and speed with which peripherals can interact with the system, and determines the thruput rate of the system.

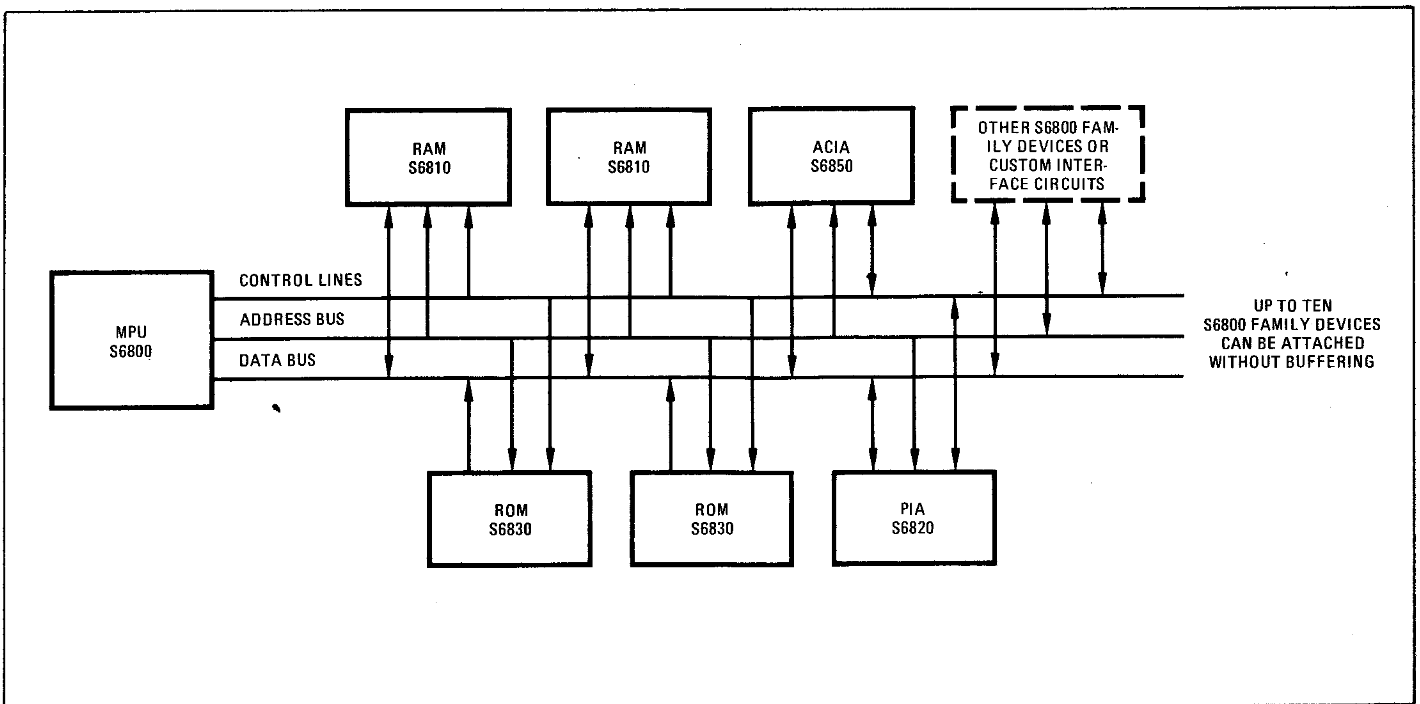
Therefore, the efficiency and versatility with which a CPU can handle its I/O – both in hardware and software – is an important criteria and is of particular concern to the user. It is in this area of I/O that the S6800 MPU excels.

- In a S6800 system, the MPU relegates most of the I/O control to such I/O interfaces as the PIA or ACIA. Each of these circuits is programmable and can interface with peripheral devices without directly involving the MPU. For example, the MPU can preprogram a PIA to either output data to the MPU or to receive it. Thereafter, the PIA circuits assume all functions of interfacing with the peripherals and the MPU never has to look at the interface until service is required. It must service interrupts from the PIA, but never needs to wait for input data to become available or for output data to be accepted. This relieves the MPU of its I/O functions, makes it more efficient in its primary task of data processing, and significantly increases system thruput.

- The I/O interfaces and memory are both located in the same address space within the S6800 system. The MPU can access any I/O device the same as a memory location – with address lines, instead of separate I/O control lines. Therefore, it can manipulate data in the I/O interface registers with the same programmed instructions as it uses for memory locations. This adds flexibility and increases system efficiency.

- The S6800 Instruction Set complements the above I/O addressing capability with specific instructions that can be used to access memory as well as I/O circuit registers and perform directly various manipulations on the data.

FIGURE 2 EXPANDING THE S6800 SYSTEM



S6800 INSTRUCTION SET

The S6800 MPU has a set of 72 basic instructions, listed in alphabetical order in Table 1. These include binary and decimal arithmetic functions, as well as logical, shift, rotate, load, store, branch, interrupt, and stack manipulation functions. Most of the instructions have several variations and most can be used with several memory addressing modes (see Table 2). Thus, the total complex of instructions available to the programmer actually is 197.

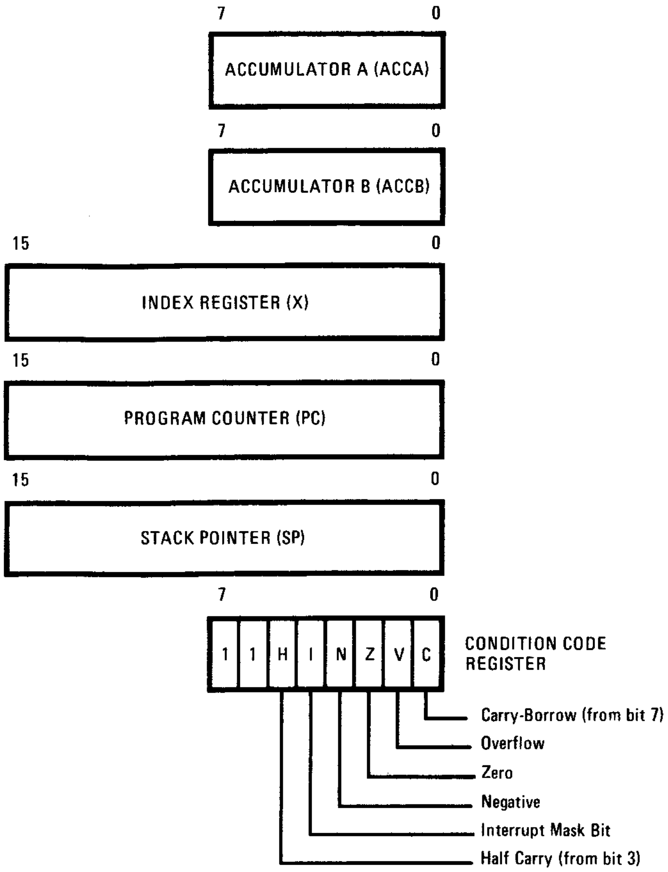
An instruction can be from one to three bytes long, depending on the addressing mode used with the instruction. The first byte always contains the operation code, which designates the kind of operation the MPU will perform. In single byte instructions no memory address is required, because the operation is performed on one of the internal MPU registers. In multiple byte instructions the second and third byte can be the operand, or a memory address for the operand. Formats for multiple byte instructions are shown in Table 2.

A noteworthy feature of the S6800 MPU is that some of the instructions can operate directly on any memory location. In other computer systems it is common that the processor fetches an operand from memory, stores it in the accumulator, then executes the operation in the ALU, and finally writes the result back into the memory. The S6800 is able to accomplish the same with only a single instruction, because it operates with any external location in the same manner as with an internal register. For example, it can directly increment or decrement the contents of a memory location. Because the MPU addresses I/O devices just like a memory location, it can do the same with registers inside the PIA or ACIA. The ASL, ASR, LSR, and ROL are other examples of instructions which operate in this manner.

TABLE 1 S6800 MICROPROCESSOR INSTRUCTION SET

ABA	Add Accumulators
ADC	Add with Carry
ADD	Add
AND	Logical And
ASL	Arithmetic Shift Left
ASR	Arithmetic Shift Right
BCC	Branch if Carry Clear
BCS	Branch if Carry Set
BEQ	Branch if Equal to Zero
BGE	Branch if Greater or Equal Zero
BGT	Branch if Greater than Zero
BHI	Branch if Higher
BIT	Bit Test
BLE	Branch if Less or Equal
BLS	Branch if Lower or Same
BLT	Branch if Less than Zero
BMI	Branch if Minus
BNE	Branch if Not Equal to Zero
BPL	Branch if Plus
BRA	Branch Always
BSR	Branch to Subroutine
BVC	Branch if Overflow Clear
BVS	Branch if Overflow Set
CBA	Compare Accumulators
CLC	Clear Carry
CLI	Clear Interrupt Mask
CLR	Clear
CLV	Clear Overflow
CMP	Compare
COM	Complement
CPX	Compare Index Register
DAA	Decimal Adjust
DEC	Decrement
DES	Decrement Stack Pointer
DEX	Decrement Index Register
EOR	Exclusive OR
INC	Increment
INS	Increment Stack Pointer
INX	Increment Index Register
JMP	Jump
JSR	Jump to Subroutine
LDA	Load Accumulator
LDS	Load Stack Pointer
LDX	Load Index Register
LSR	Logical Shift Right
NEG	Negate
NOP	No Operation
ORA	Inclusive OR Accumulator
PSH	Push Data
PUL	Pull Data
ROL	Rotate Left
ROR	Rotate Right
RTI	Return from Interrupt
RTS	Return from Subroutine
SBA	Subtract Accumulators
SBC	Subtract with Carry
SEC	Set Carry
SEI	Set Interrupt Mask
SEV	Set Overflow
STA	Store Accumulator
STS	Store Stack Register
STX	Store Index Register
SUB	Subtract
SWI	Software Interrupt
TAB	Transfer Accumulators
TAP	Transfer Accumulators to Condition Code Reg.
TBA	Transfer Accumulators
TPA	Transfer Condition Code Reg. to Accumulator
TST	Test
TSX	Transfer Stack Pointer to Index Register
TXS	Transfer Index Register to Stack Pointer
WAI	Wait for Interrupt

FIGURE 3 PROGRAM ACCESSIBLE REGISTERS



MPU REGISTERS:

Accumulators A and B – Two separate 8-bit accumulators that are used to hold operands and results of operations in the ALU.

Index Register – A 16-bit register used for memory address storage in Indexed Addressing operations.

Program Counter – A 16-bit register that holds the current program instruction address. Once the initial program starting address is loaded into the program counter, it is incremented under control of the MPU hardware.

Stack Pointer – A 16-bit register used for storage of the next available location in an external push-down/pop-up stack.

Condition Code Register – An 8-bit register that stores certain results of operations in the ALU. These bits are used as testable conditions for the conditional branch instructions. In addition, one bit position stores the interrupt mask bit and the two high order bits are unused.

MEMORY REGISTER:

EXTERNAL STACK

The MPU uses a push-down/pop-up stack that can be located anywhere in RAM and be of any convenient size. It is accessed with the stack pointer address and has several uses. First, it always stores the MPU register contents following an interrupt and return addresses during subroutine execution. Second, it can also be used by the programmer to store data during program execution.

TABLE 2 MEMORY REFERENCE INSTRUCTION FORMATS*

Immediate Addressing

OP CODE	OPERAND

OP CODE	OPERAND (HI)	OPERAND (LO)

Instruction in which the operand immediately follows the op code. The operand is one byte for all accumulator operations and two bytes for index register or stack register operations.

Direct Addressing

OP CODE	ADDRESS 0-255

A two byte instruction in which the address of the operand is contained in the second byte of the instruction. This instruction allows direct addressing of operands within the first 256 memory locations (usually a RAM location).

Extended Addressing

OP CODE	ADDRESS (HI)	ADDRESS (LO)

A three byte instruction in which the op code is followed by two bytes containing the full 16-bit memory address. This instruction can be used for addressing all 65,536 memory locations.

Indexed Addressing

OP CODE	INDEX ADDRESS

A two byte instruction whose second byte is an unsigned number, which is added to the contents of the index register. The resulting 16-bit address is then used to address the memory. The contents of the index register remain unaltered after the addition.

Relative Addressing

OP CODE	RELATIVE ADDRESS

A two byte instruction whose second byte is a signed 2's complement number which is added to the program counter. The resulting address is used to access the memory. This instruction allows the addressing of any memory location within a range of 129 bytes forward and 125 bytes back of the address contained in the program counter at the start of the instruction.

(**Accumulator and Implied Addressing** – These instructions operate directly on an MPU internal register and therefore are not concerned with memory addressing. They always are single byte instructions.)

**Instructions listed in Table 1 represent the operation codes only; in most cases they are followed by an operand or address, in the format shown in this table.*

S6800 MICROPROCESSOR

The S6800 Microprocessor (MPU) is an 8-bit parallel processor. It contains an 8-bit arithmetic unit (ALU), two 8-bit accumulators, one condition code register, and three 16-bit address storage registers, all of which are available for program use (see Figure 4). In addition, there are the following non-accessible registers: a 16-bit address incrementer/decrementer, an 8-bit temporary register and an 8-bit instruction register. There is also an instruction decode ROM and cycle control logic, interrupt and restart logic, bus control and halt logic, and a timing generator.

Within the MPU all data and address transfers between the registers, as well as to and from the ALU, are made across three internal 8-bit busses. The first is a data bus, the second is an address bus for the low order bits, and the third is an address bus for high order bits.

The MPU communicates with its external memory and all I/O devices across an 8-bit bidirectional data bus, D0 through D7, and 16 address lines, A0 through A15. The MPU can be disconnected from either bus by two control signals DBE and TSC.

MPU Operating Cycle. Instructions are executed within the MPU in incremental time periods (MPU cycles), each consisting of one $\phi 1$ clock period and one $\phi 2$ clock period. When the MPU is operating on a 1 MHz input clock, each MPU cycle is 1 microsecond long. It takes a minimum of two MPU cycles to execute an instruction.

During the $\phi 1$ period the MPU typically outputs a memory address to access (fetch) one 8-bit program instruction or data byte and then, during $\phi 2$, loads the byte into an internal register. During the next $\phi 1$ period the MPU executes the associated internal operation with the ALU and the registers. With this fetch-execute sequence an instruction may be completed in only two MPU cycles, or may require as many as 12. While the MPU is executing successive cycles, it is also common for it to overlap functions. For example, during any given clock period the MPU may be executing one instruction in the ALU or registers; while at the same time a fetch is being performed with the address in the program counter.

These internal operations of the MPU, as well as the output of address, data, and control signals, are all managed by the instruction decode and control logic. For example, to perform the execute part of any instruction, the control logic circuits generate signals that cause the ALU to perform addition, subtraction, or some Boolean logic function. These signals can also cause the contents of one register to be transferred into another, a register to be simply incremented or decremented, or some other similar function to occur. Such ALU and register operations are used to execute all of the S6800 instructions.

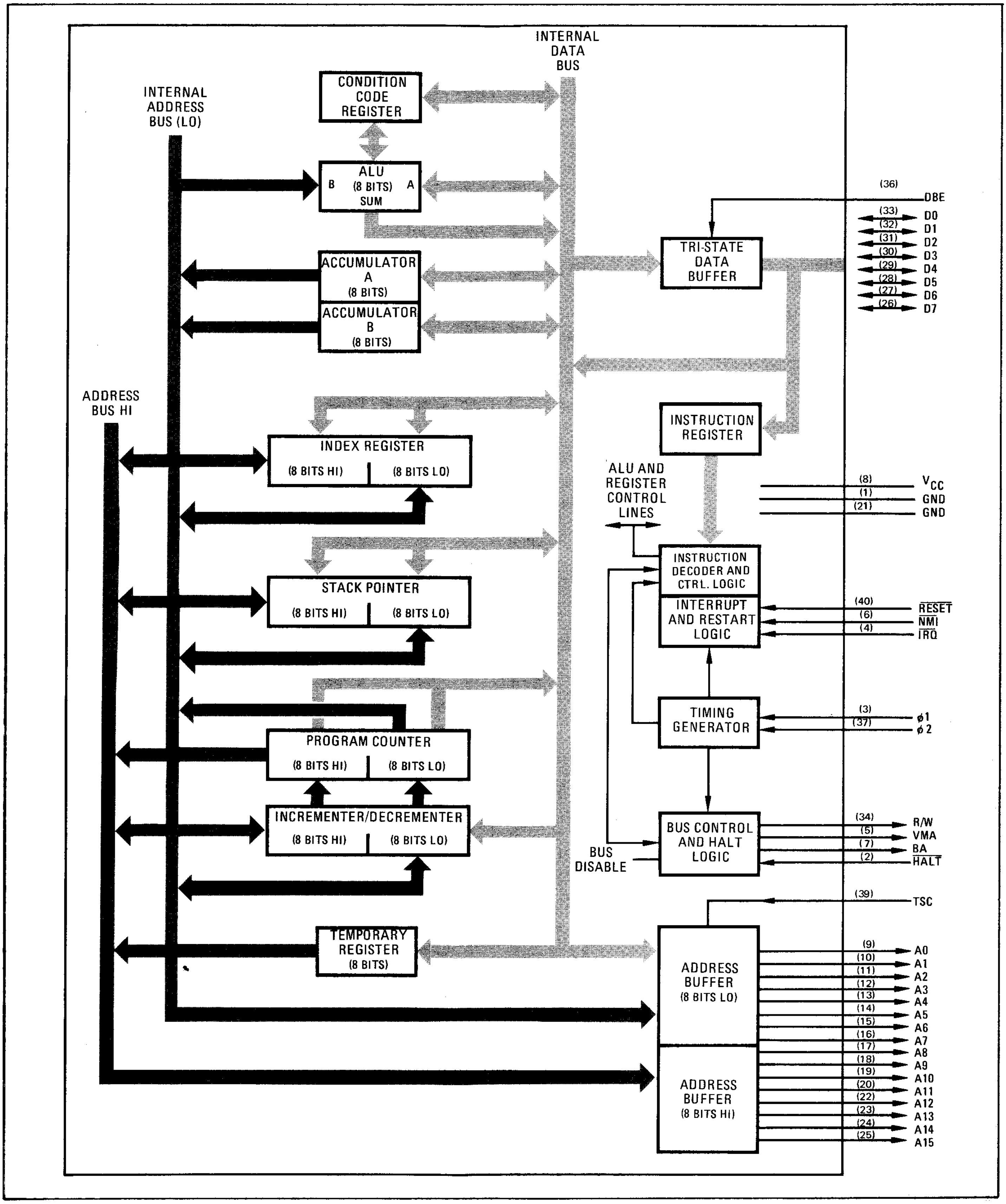
Memory Addressing Modes. During the fetch part of any MPU cycle a memory address is required in order to access a particular location in the external memory. This address is normally stored in the program counter. The program counter is 16 bits wide and therefore, can address any one of a maximum of 65,536 bytes.

At the beginning of a program sequence the MPU is initialized and the beginning address is loaded into the program counter. From there on the program counter is incremented automatically, so that at the end of any instruction cycle it stores the next instruction address. If the program contains an instruction to branch or jump to a different memory location, the op code must be followed by two bytes which load the new address into the program counter. There are, however, addressing techniques with which the jump can be accomplished by fetching only one new address byte out of the memory. These are related to the memory addressing instructions listed in Table 2.

TABLE 3 HARDWARE REGISTERS (NOT ACCESSIBLE BY PROGRAM)

Instruction Register – 8-bit register used to receive and store all program instructions input into the MPU (via the data bus lines D0-D7). **Temporary Register** – 8-bit register typically used to store the high order address bits prior to their output from the MPU onto the external address bus lines A8-A15.	**Incrementer** – 16-bit auxiliary address register, used by the MPU internal control logic, in conjunction with the program counter, to maintain and output the current program address.

FIGURE 4 BLOCK DIAGRAM OF S6800 MICROPROCESSOR



For example, if the destination of a branch is within 129 locations forward of 125 locations back of the current program counter contents, Relative Addressing can be used. In this mode only the op code and one signed 8-bit byte is fetched from the memory and is added to the program counter contents.

In Indexed Addressing, a single byte is added to the contents of the index register and the result is transferred into the program counter. Thus, the above addressing variations can be used to reduce the number of bytes that need be fetched to generate a new address. This reduces the number of MPU cycles and speeds up program execution.

The various addressing modes can also be used in a similar manner to generate the source or destination addresses for data.

TABLE 4 S6800 INTERRUPTS

Nonmaskable Interrupt (NMI) – initiated by a low-going signal on the $\overline{\text{NMI}}$ line to the MPU; always interrupts the MPU – even while another interrupt is being processed and the interrupt mask bit is set. Therefore, NMI can be considered to the highest priority interrupt. It causes the following sequence of events:

1. At the completion of the instruction being executed, the contents of the program accessible registers (Figure 3) are stored in the stack.
2. The interrupt mask bit is set.
3. Starting with its next cycle, the MPU accesses locations FFFC and FFFD in the memory and loads the contents into the program counter.

Interrupt Request (IRQ) – initiated by a logic low signal on the $\overline{\text{IRQ}}$ line; interrupts the MPU as long as the interrupt mask bit is not set. It causes the following sequence of events:

1. At the completion of the instruction being executed, the interrupt mask bit is tested. If the bit is set the interrupt must wait; if it is not set, contents of the program accessible registers are stored in the stack.
2. The interrupt mask bit is set.
3. Starting with the next cycle, the MPU accesses locations FFF8 and FFF9 in the memory and loads the contents into the program counter.

Software Interrupt (SWI) – initiated by the SWI instruction and causes the following sequence of events:

1. Contents of the program accessible registers are stored in the stack.
2. The interrupt mask bit is set.
3. Starting with the next cycle, the MPU accesses locations FFFA and FFFB in the memory and loads the contents into the program counter.

Reset – initiated by a positive going edge on the $\overline{\text{RESET}}$ line to the MPU. It causes the following sequence of events:

1. All program accessible registers are cleared and other circuits in the MPU are initialized.
2. The interrupt mask bit is set.
3. Starting with the next cycle, the MPU accesses locations FFFE and FFFF in the memory and loads the contents into the program counter.

Wait (WAI) – an instruction that causes the MPU to stop all processing and wait for a hardware interrupt. This instruction is not an interrupt in itself because it does not cause branching to any memory address, however, it does cause contents of the program accessible registers to be stored into the stack, in preparation for an interrupt.

Interrupts. The S6800 MPU can be interrupted by any of several signals and program instructions, each of which initiates a different sequence in the MPU. Including the Reset signal, there are four interrupts – three hardware interrupts (signal lines connected to the MPU) and one software interrupt (SWI instruction). Each is described separately in Table 4.

All interrupts are vectored – they cause the MPU to automatically access a predetermined location in the memory and fetch a branch address of the routine or program to which the MPU is to go to service the interrupt. All interrupts except Reset also cause the contents of each program accessible MPU register (with the exception of the stack pointer) to be transferred to the external stack and thus be saved for later processing. The IRQ interrupt is also maskable – it cannot interrupt the MPU as long as bit 4 in the condition code register is set.

APPLICATIONS

The following five figures show various S6800 applications and system interconnections. Because the specific applications of microcomputers are so many and diverse, the figures are intended as general models for systems, in which the particular combination of devices, details of their interconnections, and control line utilization are left up to the user. Refer to the following data sheets for details about each device in the S6800 family.

FIGURE 5 DATA COMMUNICATIONS SYSTEM

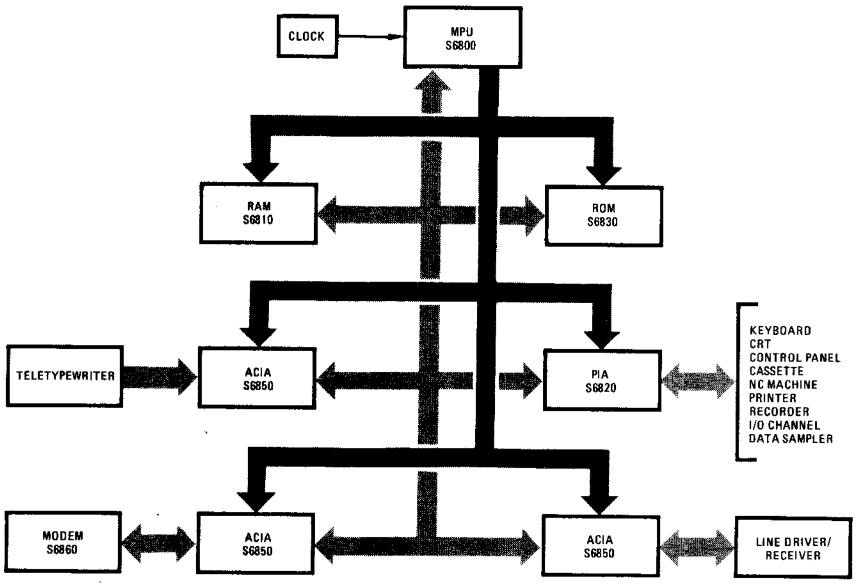


FIGURE 6 DATA ACQUISITION SYSTEM

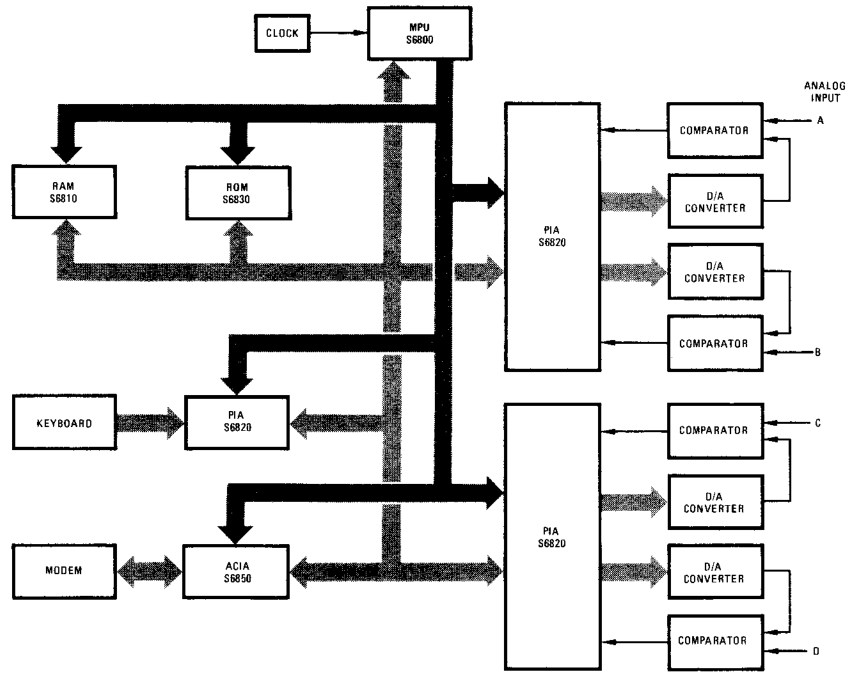


FIGURE 7 TRAFFIC CONTROL SYSTEM

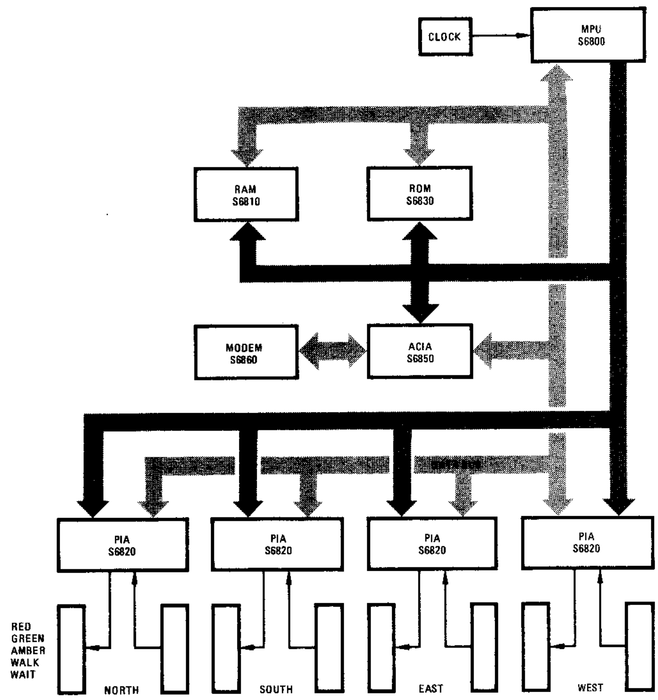


FIGURE 8 CRT DISPLAY SYSTEM

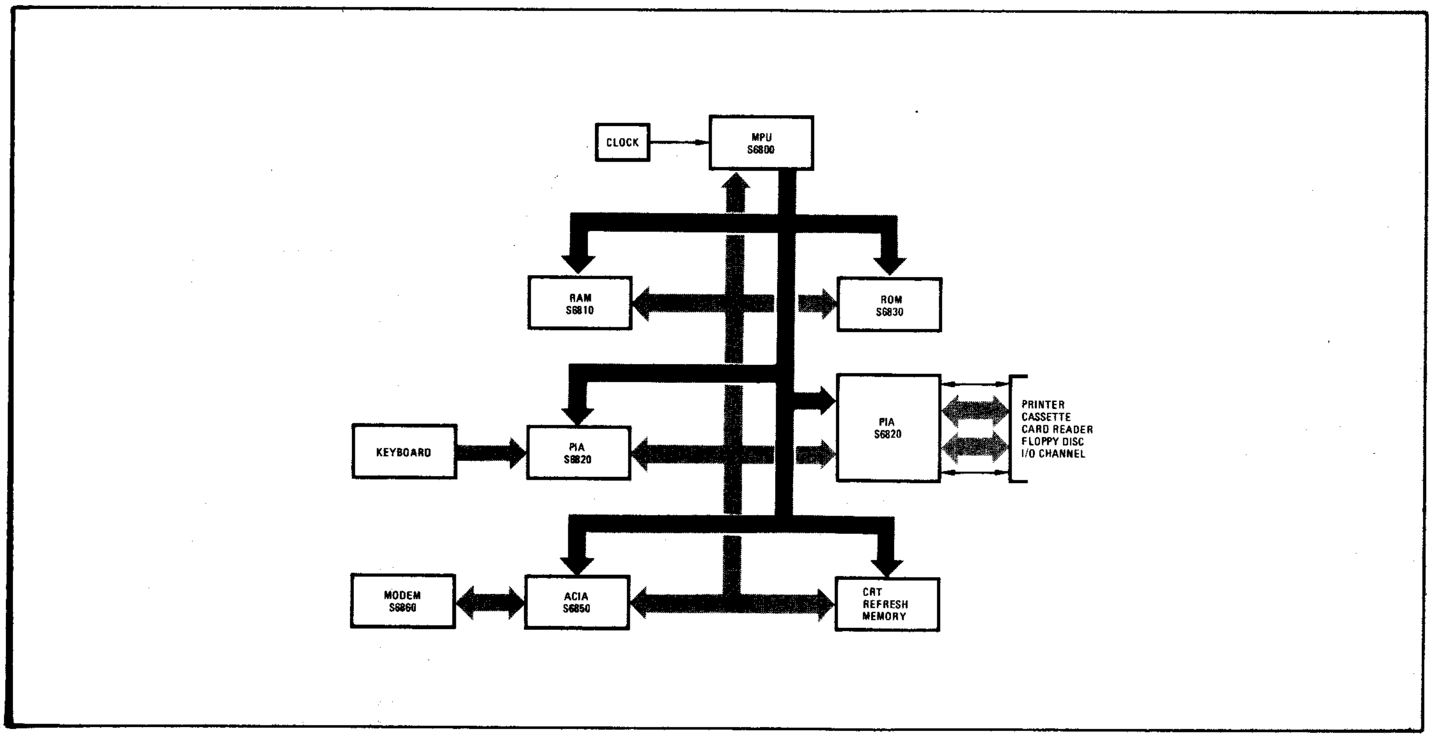
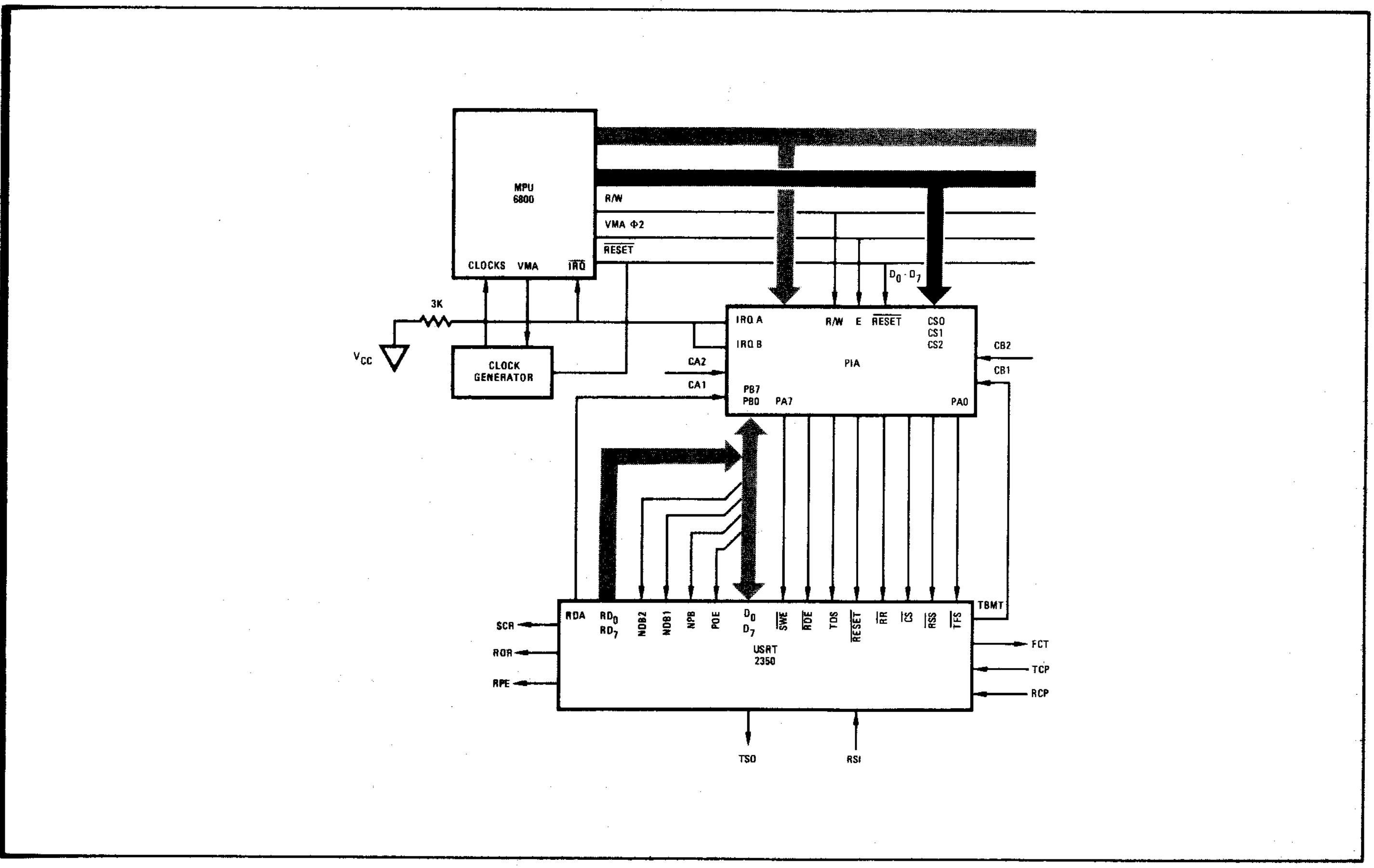


FIGURE 9 SCHEMATIC DIAGRAM FOR INTERCONNECTING S2350 USRT TO THE S6800 MPU

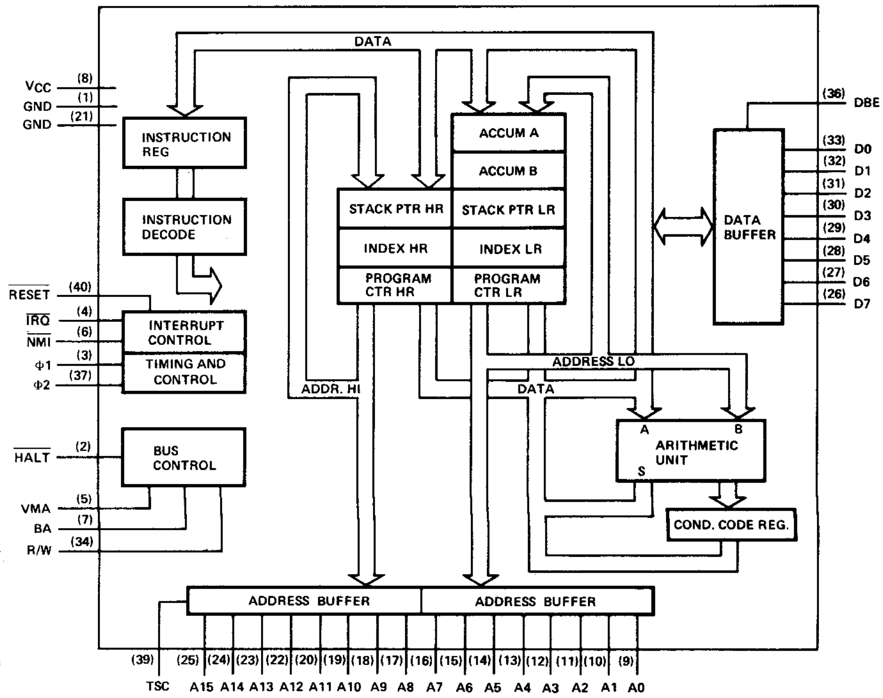


S6800

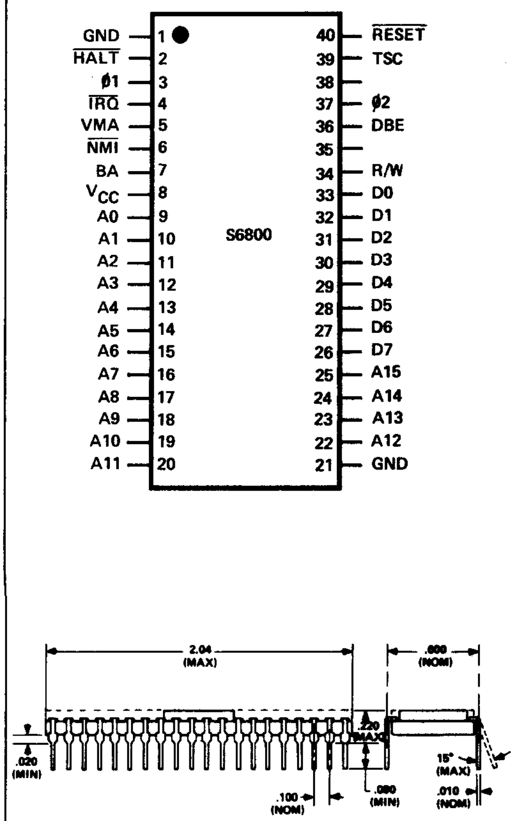
8-BIT
MICROPROCESSOR

AMI
AMERICAN MICROSYSTEMS, INC.

ADVANCED PRODUCT DESCRIPTION



BLOCK DIAGRAM



PIN/PACKAGE CONFIGURATION

FEATURES

- Eight-Bit Parallel Processing
- Bi-Directional Data Bus
- Sixteen-Bit Address Bus – 65536 Bytes of Addressing
- 72 Instructions – Variable Length
- Seven Addressing Modes – Direct, Relative, Immediate, Indexed, Extended, Implied and Accumulator
- Variable Length Stack
- Vectored Restart
- 2 Microsecond Instruction Execution
- Maskable Interrupt Vector
- Separate Non-Maskable Interrupt – Internal Registers Saved in Stack
- Six Internal Registers – Two Accumulators, Index Register, Program Counter, Stack Pointer and Condition Code Register
- Direct Memory Access (DMA) and Multiple Processor Capability
- Clock Rates as High as 1 MHz
- Simple Bus Interface Without TTL
- Halt and Single Instruction Execution Capability

INC

ABSOLUTE MAXIMUM RATINGS

Supply Voltage V_{CC}	–0.3 to +7.0V
Input Voltage V_{in}	–0.3 to +7.0V
Operating Temperature Range T_A	0 to +70°C
Storage Temperature Range T_{stg}	–55 to +150°C

DC (STATIC) CHARACTERISTICS

(V_{CC} = 5.0 V ± 5%, T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min.	Typ.	Max.	Unit
Input High Voltage (Normal Operating Levels) Logic	V_{IH}	+ 2.4	–	V_{CC}	Vdc
$\phi1,\phi2$	V_{IHC}	V_{CC} –0.3	–	V_{CC} +0.1	
Input Low Voltage (Normal Operating Levels) Logic	V_{IL}	–0.3	–	+ 0.4	Vdc
$\phi1,\phi2$	V_{ILC}	–0.1	–	+0.3	
Clock Overshoot/Undershoot – Input High Level	V_{OS}	V_{CC} –0.5	–	V_{CC} +0.5	Vdc
– Input Low Level		–0.5	–	+0.5	
Input High Threshold Voltage Reset, NMI, Halt, IRQ, Data	V_{IHT}	+ 2.0	–	–	Vdc
Input Low Threshold Voltage Reset, NMI, Halt, IRQ, Data	V_{ILT}	–	–	+ 0.8	Vdc
Input Leakage Current (V_{in} = 0 to 5.25 V, V_{CC} = 5.25V) Logic*	I_{in}	–	–	2.5	μAdc
$\phi1,\phi2$		–	–	100	
Three-State (Off State) Input Current (V_{in} = 0.4 to 2.4 V, V_{CC} = max) Data	I_{TSI}	–	–	10	μAdc
A0-A15, R/W		–	–	100	
Output High Voltage (I_{Load} = –100 μAdc, V_{CC} = min)	V_{OH}	+ 2.4	–	–	Vdc
Output Low Voltage (I_{Load} = 1.6 mAdc, V_{CC} = min)	V_{OL}	–	–	+ 0.4	Vdc
Power Dissipation	P_D	–	0.600	1.2	W
Capacitance** (V_{in} = 0, T_A = 25°C, f = 1.0 MHz) Logic	C_{in}	–	–	10	pF
Data, TSC		–	–	15	
$\phi1,\phi2$		80	120	160	
A0-A15, R/W	C_{out}	–	–	12	pF

*Except IRQ and NMI, which require 3 kΩ pullup load resistors for wire-OR capability at optimum operation.
**Capacitances are periodically sampled rather than 100% tested.

AC (DYNAMIC) CHARACTERISTICS

(V_{CC} = 5.0 volt ± 5%, T_A = 25°C unless otherwise noted.)

Characteristic	Symbol	Min.	Typ	Max.	Unit
Frequency of Operation	f	0.1	–	1.0	MHz
Clock Timing for 1-MHz Operation (Figure 1) (C_{clock} = 200 pF) Cycle Time	t_{cyc}	1.0	–	10	μs
Clock Pulse Width (Measured at V_{CC} –0.3 V) φ1	PWφH	430	–	4500	ns
φ2		450	–	4500	
Total φ1 and φ2 UP Time	t_{ut}	940	–	–	ns
Rise and Fall Times φ1,φ2 (Measured between 0.3 V and V_{CC} –0.3 V)	t_r, t_f	5.0	–	50	ns
Delay Time or Clock Overlap (Measured at 0.5 V)	t_d	0	–	9100	ns
Overshoot/Undershoot Duration	t_{os}	0	–	40	ns

READ/WRITE TIMING

Figures 2 and 3, f = 1.0 MHz, Loading = 130 pF and one TTL Load except VMA and BA Loading = 30 pF and one

Characteristic	Symbol	Min.	Typ	Max.	Unit
Read/Write Setup Time from MPU	T_{ASR}	–	100	300	ns
Address Setup Time from MPU	T_{ASC}	–	200	300	ns
Memory Read Access Time t_{cyc} – (T_{ASC} + T_{DSU} + t_r)	T_{ACC}	–	–	575	ns
Data Setup Time	T_{DSU}	100	–	–	ns
Address Setup Time from MPU for VMA	T_{VSC}	–	150	300	ns
Data Hold Time	T_H	10	30	–	ns
Enable High Time for DBE Input	T_{EH}	470	–	–	ns
Data Setup Time from MPU	T_{ASD}	–	150	200	ns

FIGURE 1 – CLOCK TIMING WAVEFORM

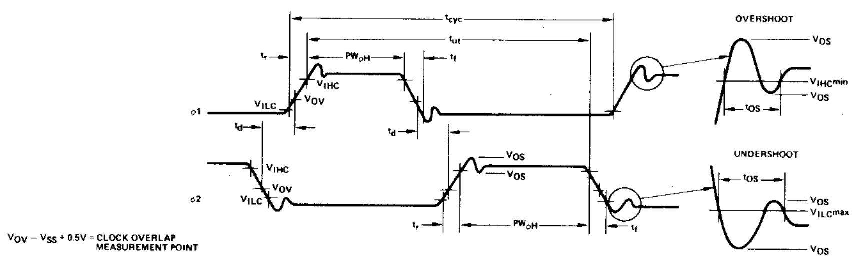


FIGURE 2 – READ DATA FROM MEMORY OR PERIPHERALS

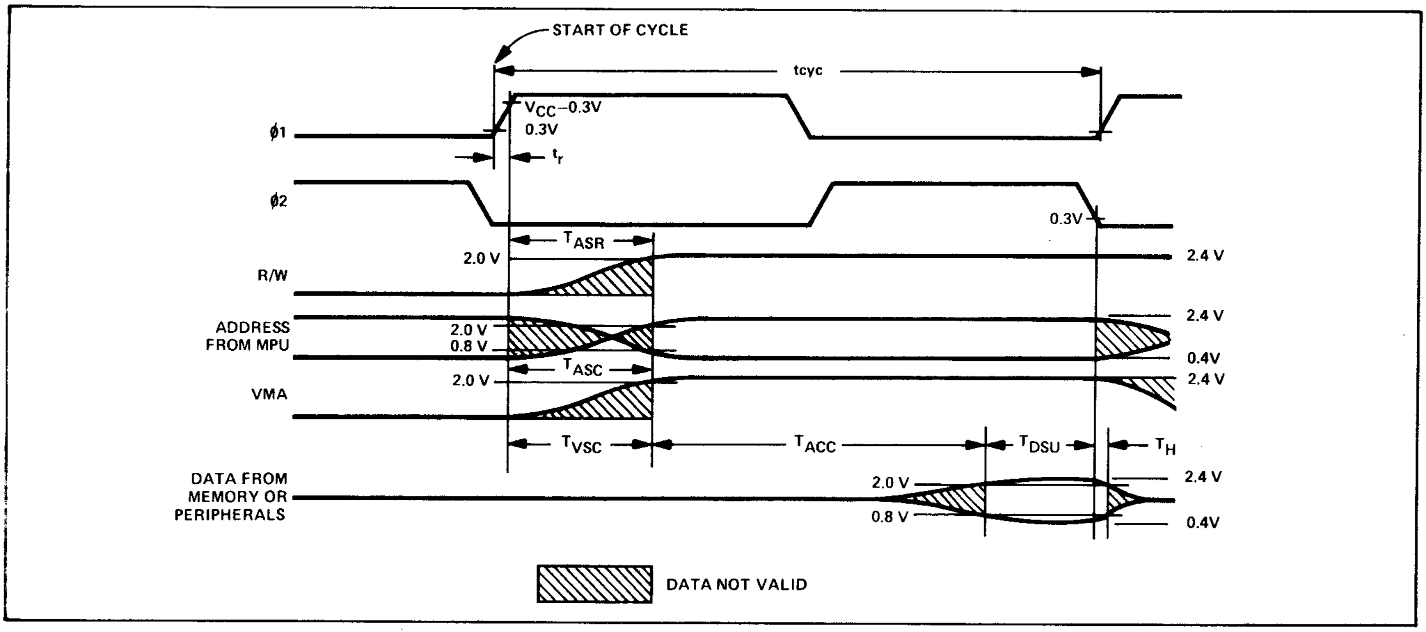
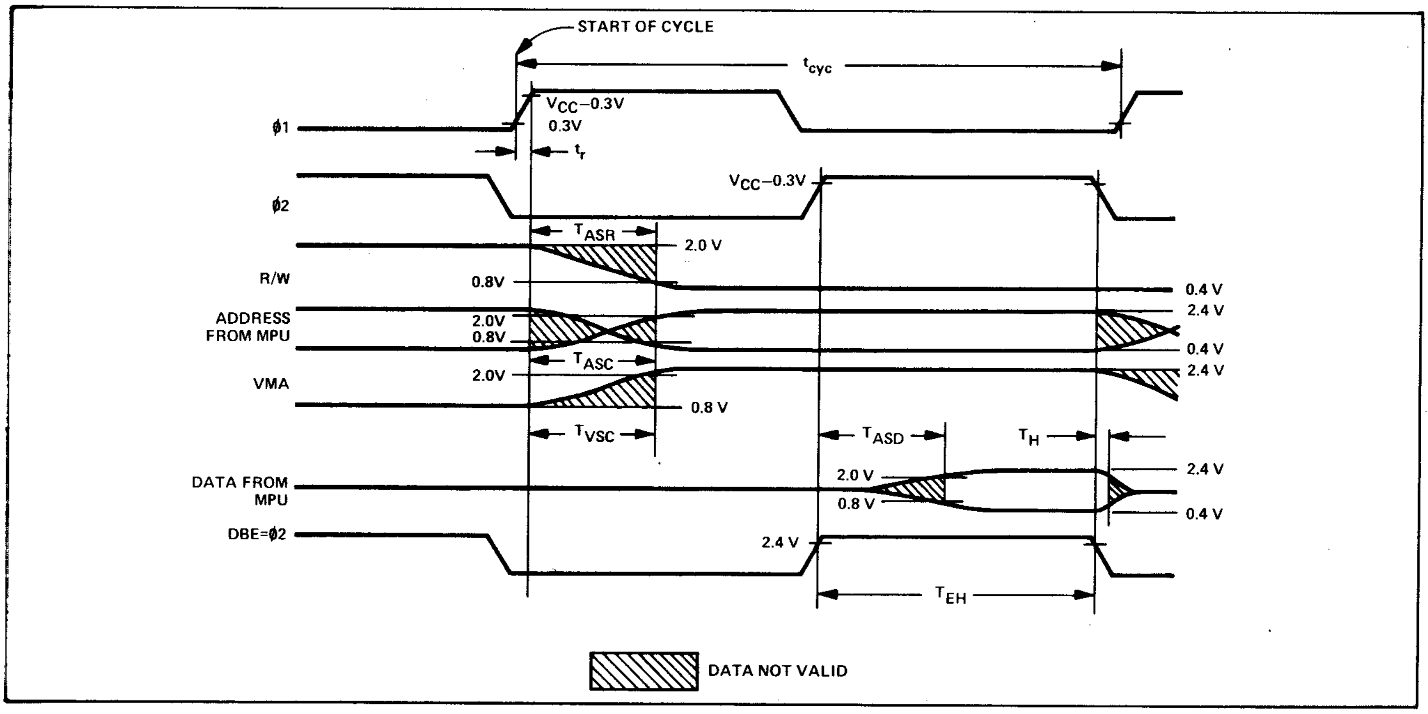


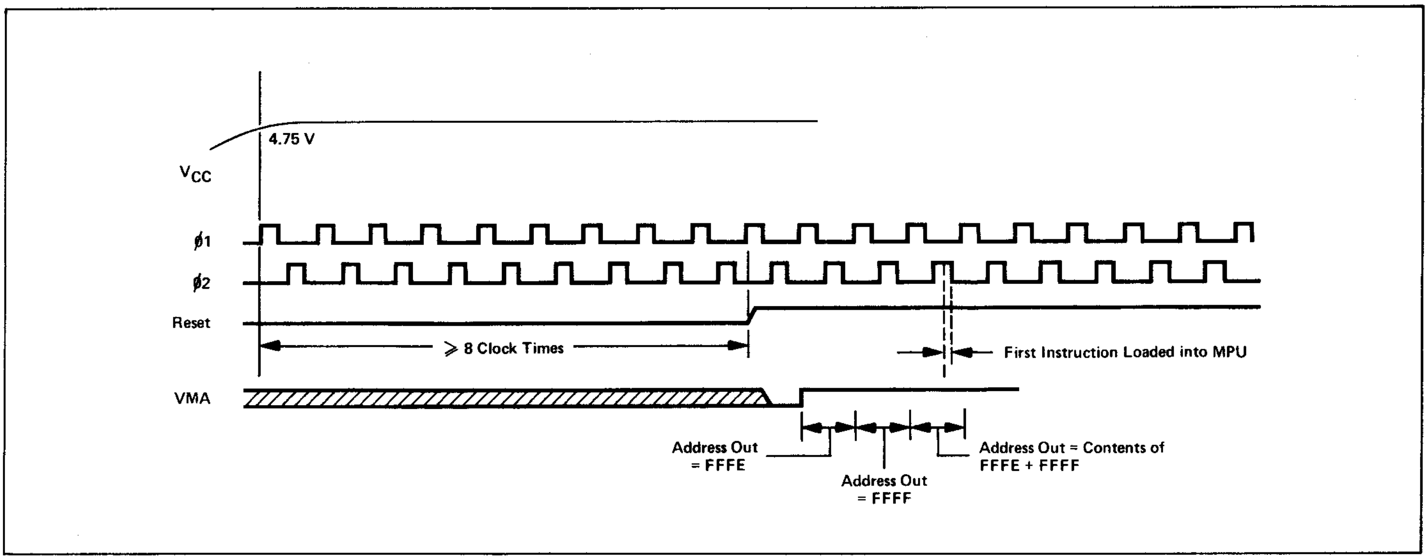
FIGURE 3 – WRITE DATA IN MEMORY OR PERIPHERALS



INTERFACE DESCRIPTION

Label	Pin	Function
$\phi 1$ $\phi 2$	(3) (37)	**Clocks Phase One and Phase Two** – Two pins are used for a two-phase non-overlapping clock that runs at the V_{CC} voltage level.
$\overline{\text{RESET}}$	(40)	**$\overline{\text{Reset}}$** – This input is used to reset and start the MPU from a power down condition, resulting from a power failure or an initial start-up of the processor. If a positive edge is detected on the input, this will signal the MPU to begin the restart sequence. This will start execution of a routine to initialize the processor from its reset condition. All the higher order address lines will be forced high. For the restart, the last two (FFFE, FFFF) locations in memory will be used to load the program that is addressed by the program counter. During the restart routine, the interrupt mask bit is set and must be reset before the MPU can be interrupted by $\overline{\text{IRQ}}$. $\overline{\text{Reset}}$ must be held low for at least eight clock periods after V_{CC} reaches 4.75 volts (Figure 4). If $\overline{\text{Reset}}$ goes high prior to the leading edge of $\phi 2$, on the next $\phi 1$ the first restart memory vector address (FFFE) will appear on the address lines. This location should contain the higher order eight bits to be stored into the program counter. Following, the next address FFFF should contain the lower order eight bits to be stored into the program counter.

FIGURE 4
INITIALIZATION OF MPU AFTER RESTART



VMA	(5)	**Valid Memory Address** – This output indicates to peripheral devices that there is a valid address on the address bus. In normal operation, this signal should be utilized for enabling peripheral interfaces such as the PIA and ACIA. This signal is not three-state. One standard TTL load and 30 pF may be directly driven by this active high signal.

Label	Pin	Function
A0 • • • A15	(9) (25)	**Address Bus** – Sixteen pins are used for the address bus. The outputs are three-state bus drivers capable of driving one standard TTL load and 130 pF. When the output is turned off, it is essentially an open circuit. This permits the MPU to be used in DMA applications.
TSC	(39)	**Three-State Control** – This input causes all of the address lines and the Read/Write line to go into the off or high impedance state. This state will occur 500 ns after TSC = 2.4 V. The Valid Memory Address and Bus Available signals will be forced low. The data bus is not affected by TSC and has its own enable (Data Bus Enable). In DMA applications, the Three-State Control line should be brought high on the leading edge of the Phase One Clock. The $\phi 1$ clock must be held in the high state and the $\phi 2$ in the low state for this function to operate properly. The address bus will then be available for other devices to directly address memory. Since the MPU is a dynamic device, it can be held in this state for only 5.0 μs or destruction of data will occur in the MPU.
D0 • • D7	(33) (26)	**Data Bus** – Eight pins are used for the data bus. It is bi-directional, transferring data to and from the memory and peripheral devices. It also has three-state output buffers capable of driving one standard TTL load at 130 pF.
DBE	(36)	**Data Bus Enable** – This input is the three-state control signal for the MPU data bus and will enable the bus drivers when in the high state. This input is TTL compatible; however in normal operation, it can be driven by the phase two clock. During an MPU read cycle, the data bus drivers will be disabled internally. When it is desired that another device control the data bus such as in Direct Memory Access (DMA) applications, DBE should be held low.
R/W	(34)	**Read/Write** – This TTL compatible output signals the peripherals and memory devices whether the MPU is in a Read (high) or Write (low) state. The normal standby state of this signal is Read (high). Three-State Control going high will turn Read/Write to the off (high-impedance) state. Also, when the processor is halted, it will be in the off state. This output is capable of driving one standard TTL load and 130 pF.
$\overline{\text{HALT}}$	(2)	**$\overline{\text{Halt}}$** – When this input is in the low state, all activity in the machine will be halted. This input is level sensitive. In the halt mode, the machine will stop at the end of an instruction, Bus Available will be at a one level, Valid Memory Address will be at a zero, and all other three-state lines will be in the three-state mode. Transition of the $\overline{\text{Halt}}$ line must not occur during the last 250 ns of phase one. To insure single instruction operation, the $\overline{\text{Halt}}$ line must go high for one Phase One Clock cycle.
BA	(7)	**Bus Available** – The Bus Available signal will normally be in the low state; when activated, it will go to the high state indicating that the microprocessor has stopped and that the address bus is available. This will occur if the $\overline{\text{Halt}}$ line is in the low state or the processor is in the WAIT state as a result of the execution of a WAIT instruction. At such time, all three-state output drivers will go to their off state and other outputs to their normally inactive level. The processor is removed from the WAIT state by the occurrence of a maskable (mask bit I = 0)or nonmaskable interrupt. This output is capable of driving one standard TTL load and 30 pF.

Label	Pin	Function
$\overline{\text{IRQ}}$	(4)	**Interrupt Request** – This level sensitive input requests that an interrupt sequence be generated within the machine. The processor will wait until it completes the current instruction that is being executed before it recognizes the request. At that time, if the interrupt mask bit in the Condition Code Register is not set, the machine will begin an interrupt sequence. The Index Register, Program Counter, Accumulators, and Condition Code Register are stored away on the stack. Next the MPU will respond to the interrupt request by setting the interrupt mask bit high so that no further interrupts may occur. At the end of the cycle, a 16-bit address will be loaded that points to a vectoring address which is located in memory locations FFF8 and FFF9. An address loaded at these locations causes the MPU to branch to an interrupt routine in memory. The $\overline{\text{Halt}}$ line must be in the high state for interrupts to be recognized. The $\overline{\text{IRQ}}$ has a high impedance pullup device internal to the chip; however a 3 kΩ external resistor to V_{CC} should be used for wire-OR and optimum control of interrupts.
$\overline{\text{NMI}}$	(6)	**Non-Maskable Interrupt** – A low-going edge on this input requests that a non-mask interrupt sequence be generated within the processor. As with the Interrupt Request signal, the processor will complete the current instruction that is being executed before it recognizes the $\overline{\text{NMI}}$ signal. The interrupt mask bit in the Condition Code Register has no effect on $\overline{\text{NMI}}$. The Index Register, Program Counter, Accumulators, and Condition Code Register are stored away in the stack. At the end of the cycle, a 16-bit address will be loaded that points to a vectoring address which is located in memory locations FFFC and FFFD. An address loaded at these locations causes the MPU to branch to a non-maskable interrupt routine in memory. $\overline{\text{NMI}}$ has a high impedance pullup resistor internal to the chip; however a 3 kΩ external resistor to V_{CC} should be used for wire-OR and optimum control of interrupts. Inputs $\overline{\text{IRQ}}$ and $\overline{\text{NMI}}$ are hardware interrupt lines that are acknowledged during $\phi 2$ and will start the interrupt routine on the $\phi 1$ following the completion of an instruction.

INTERRUPTS – As outlined in the interface description the S6800 requires a 16-bit vector address to indicate the location of routines for Restart, Non-maskable Interrupt, and Maskable Interrupt. Additionally an address is required for the Software Interrupt Instruction (SWI). The processor assumes the uppermost eight memory locations, FFF8 – FFFF, are assigned as interrupt vector addresses as defined in Figure 5.

After completing the current instruction execution the processor checks for an allowable interrupt request via the $\overline{\text{IRQ}}$ or $\overline{\text{NMI}}$ inputs as shown by the simplified flow chart in Figure 6. Recognition of either external interrupt request or a Wait for Interrupt (WAI) or Software Interrupt (SWI) instruction causes the contents of the Index Register, Program Counter, Accumulators and Condition Code Register to be transferred to the stack as shown in Figure 7.

FIGURE 5 **MEMORY MAP FOR INTERRUPT VECTORS**

Vector MS	Vector LS	Description
FFFE	FFFF	Restart
FFFC	FFFD	Non-maskable Interrupt
FFFA	FFFB	Software Interrupt
FFF8	FFF9	Interrupt Request

FIGURE 6 – MPU FLOW CHART

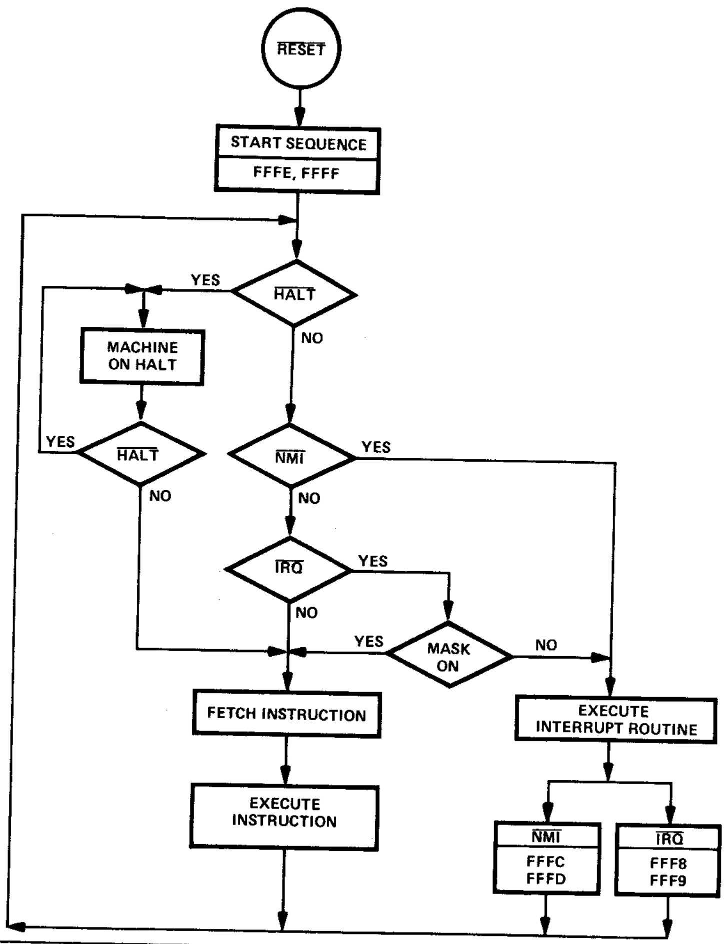
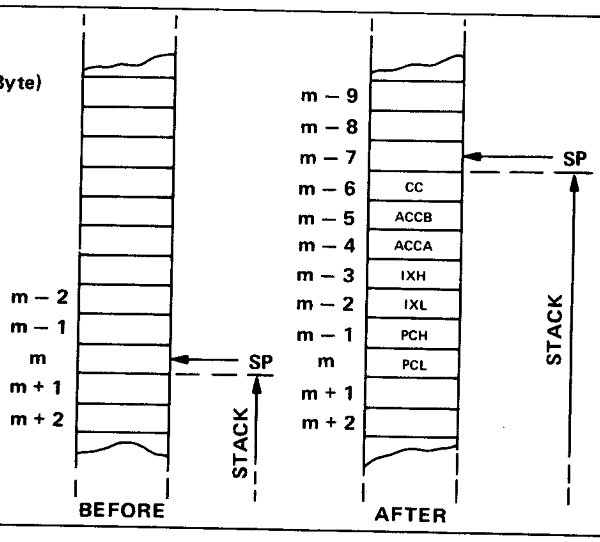


FIGURE 7 – SAVING THE STATUS OF THE MICROPROCESSOR IN THE STACK

SP = Stack Pointer
CC = Condition Codes (Also called the Processor Status Byte)
ACCB = Accumulator B
ACCA = Accumulator A
IXH = Index Register, Higher Order 8 Bits
IXL = Index Register, Lower Order 8 Bits
PCH = Program Counter, Higher Order 8 Bits
PCL = Program Counter, Lower Order 8 Bits



MPU REGISTERS

The MPU has three 16-bit registers and three 8-bit registers available for use by the programmer.

Program Counter – The program counter is a two byte (16-bits) register that points to the current program address.

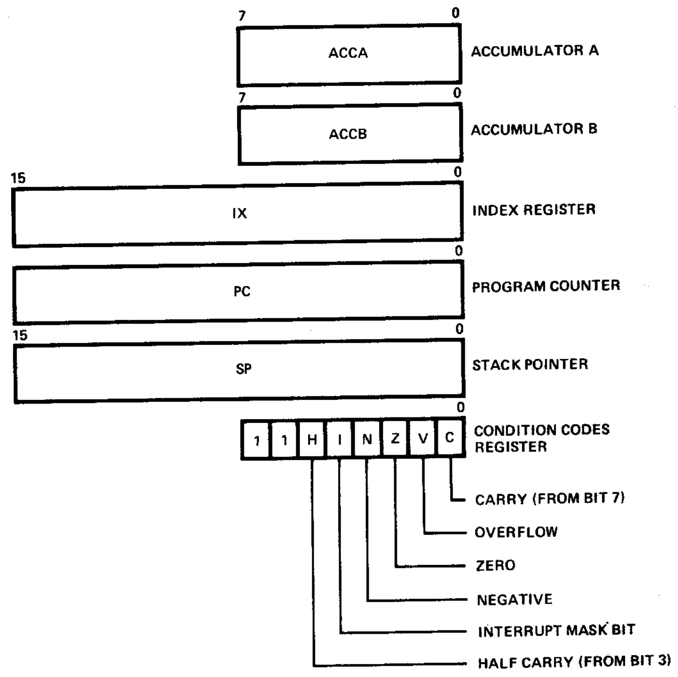
Stack Pointer – The stack pointer is a two byte register that contains the address of the next available location in an external push-down/pop-up stack. This stack is normally a random access Read/Write memory that may have any location (address) that is convenient. In those applications that require storage of information in the stack when power is lost, the stack must be non-volatile.

Index Register – The index register is a two byte register that is used to store data or a sixteen bit memory address for the Indexed mode of memory addressing.

Accumulators – The MPU contains two 8-bit accumulators that are used to hold operands and results from the arithmetic logic unit (ALU).

Condition Code Register – The condition code register indicates the results of an Arithmetic Logic Unit operation: Negative (N), Zero (Z), Overflow (V), Carry from bit 7 (C), and half carry from bit 3 (H). These bits of the Condition Code Register are used as testable conditions for the conditional branch instructions. Bit 4 is the interrupt mask bit (I). The unused bits of the Condition Code Register (b6 and b7) are ones.

FIGURE 8 – PROGRAMMING MODEL OF THE MICROPROCESSOR



MPU ADDRESSING MODES

The S6800 eight-bit microprocessing unit has seven address modes that can be used by a programmer, with the addressing mode a function of both the type of instruction and the coding within the instruction. A summary of the addressing modes for a particular instruction can be found in Figure 9 along with the associated instruction execution time that is given in machine cycles. With a clock frequency of 1 MHz, these times would be microseconds.

ACCUMULATOR ADDRESSING (ACCX)

OP CODE

A single byte instruction addressing operands only in accumulator A or accumulator B.

IMPLIED ADDRESSING

OP CODE

Single byte instruction where the operand address is implied by the instruction definition (i.e., Stack Pointer, Index Register or Condition Register).

IMMEDIATE ADDRESSING

OP CODE	IMMEDIATE OPERAND

HIGHER	IMMEDIATE OPERAND	IMMEDIATE OPERAND LOWER

Two or three byte instructions with an eight or sixteen bit operand respectively. For accumulator operations the eight bit operand is contained in the second byte of a two byte instruction. For Index Register operations (e.g. LDX) sixteen bit operand is contained in the second and third byte of a three byte instruction.

DIRECT ADDRESSING

OP CODE	ADDRESS 0-255

Two byte instructions with the address of the operand contained in the second byte of the instruction. This format allows direct addressing of operands within the first 256 memory locations.

EXTENDED ADDRESSING

OP CODE	ADDRESS HIGHER	ADDRESS LOWER

Three byte instructions with the higher eight bits of the operand address contained in the second byte and the lower eight bits of address contained in the third byte of the instruction. This format allows direct addressing of all 65,536 memory locations.

INDEXED ADDRESSING

OP CODE	INDEX ADDRESS

Two byte instructions where the 8 bit unsigned address contained in the second byte of the instruction is added to the sixteen bit Index Register resulting in a sixteen bit effective address. The effective address is stored in a temporary register and the contents of the Index Register are unchanged.

RELATIVE ADDRESSING

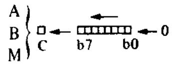
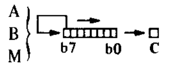
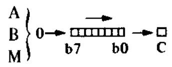
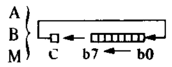
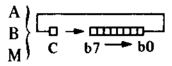
OP CODE	RELATIVE ADDRESS

Two byte instructions where the relative address contained in the second byte of the instruction is added to the sixteen bit program counter plus two. The relative address is interpreted as a two's complement number allowing relative addressing within a range of −125 to +129 bytes of the present instruction.

FIGURE 9 – S6800 INSTRUCTION SET

		Addressing Mode																		Condition Reg					
		Implied			Immediate			Direct			Extended			Indexed			Relative			Boolean/Arith	5	4	3	2	1	0
Instruction	Mnemonic	OP	MC	PB	OP	MC	PB	OP	MC	PB	OP	MC	PB	OP	MC	PB	OP	MC	PB	Operation	H	I	N	Z	V	C
Load accumulator	LDAA				86	2	2	96	3	2	B6	4	3	A6	5	2				M → A	•	•	↕	↕	R	•
	LDAB				C6	2	2	D6	3	2	F6	4	3	E6	5	2				M → B	•	•	↕	↕	R	•
Load stack pointer	LDS				8E	3	3	9E	4	2	BE	5	3	AE	6	2				M → SP_H, (M + 1) → SP_L	•	•	9	↕	R	•
Load index register	LDX				CE	3	3	DE	4	2	FE	5	3	EE	6	2				M → X_H, (M + 1) → X_L	•	•	9	↕	R	•
Store accumulator	STAA							97	4	2	B7	5	3	A7	6	2				A → M	•	•	↕	↕	R	•
	STAB							D7	4	2	F7	5	3	E7	6	2				B → M	•	•	↕	↕	R	•
Store stack pointer	STS							9F	5	2	BF	6	3	AF	7	2				SP_H → M, SP_L → (M + 1)	•	•	9	↕	R	•
Store index register	STX							DF	5	2	FF	6	3	EF	7	2				X_H → M, X_L → (M + 1)	•	•	9	↕	R	•
Transfer accumulators	TAB	16	2	1																A → B	•	•	↕	↕	R	•
	TBA	17	2	1																B → A	•	•	↕	↕	R	•
Transfer Acc. to cond. reg.	TAP	06	2	1																A → CCR	Note 12					
Transfer cond. reg. to Acc.	TPA	07	2	1																CCR → A	•	•	•	•	•	•
Transfer stck ptr to index	TSX	30	4	1																SP + 1 → X	•	•	•	•	•	•
Transfer index to stck ptr	TXS	35	4	1																X – 1 → SP	•	•	•	•	•	•
Pull data	PULA	32	4	1																SP + 1 → SP, M_{SP} → A	•	•	•	•	•	•
	PULB	33	4	1																SP + 1 → SP, M_{SP} → B	•	•	•	•	•	•
Push data	PSHA	36	4	1																A → M_{SP}, SP – 1 → SP	•	•	•	•	•	•
	PSHB	37	4	1																B → M_{SP}, SP – 1 → SP	•	•	•	•	•	•
Add accumulators	ABA	1B	2	1																A + B → A	↕	•	↕	↕	↕	↕
Add	ADDA				8B	2	2	9B	3	2	BB	4	3	AB	5	2				A + M → A	↕	•	↕	↕	↕	↕
	ADDB				CB	2	2	DB	3	2	FB	4	3	EB	5	2				B + M → B	↕	•	↕	↕	↕	↕
Add with carry	ADCA				89	2	2	99	3	2	B9	4	3	A9	5	2				A + M + C → A	↕	•	↕	↕	↕	↕
	ADCB				C9	2	2	D9	3	2	F9	4	3	E9	5	2				B + M + C → B	↕	•	↕	↕	↕	↕
Subtract accumulators	SBA	10	2	1																A – B → A	•	•	↕	↕	↕	↕
Subtract	SUBA				80	2	2	90	3	2	B0	4	3	A0	5	2				A – M → A	•	•	↕	↕	↕	↕
	SUBB				C0	2	2	D0	3	2	F0	4	3	E0	5	2				B – M → B	•	•	↕	↕	↕	↕
Subtract with carry	SBCA				82	2	2	92	3	2	B2	4	3	A2	5	2				A – M – C → A	•	•	↕	↕	↕	↕
	SBCB				C2	2	2	D2	3	2	F2	4	3	E2	5	2				B – M – C → B	•	•	↕	↕	↕	↕
Increment	INCA	4C	2	1																A + 1 → A	•	•	↕	↕	5	•
	INCB	5C	2	1																B + 1 → B	•	•	↕	↕	5	•
	INC										7C	6	3	6C	7	2				M + 1 → M	•	•	↕	↕	5	•
Increment stack pointer	INS	31	4	1																SP + 1 → SP	•	•	•	•	•	•
Increment index reg.	INX	08	4	1																X + 1 → X	•	•	•	↕	•	•
Decrement	DECA	4A	2	1																A – 1 → A	•	•	↕	↕	4	•
	DECB	5A	2	1																B – 1 → B	•	•	↕	↕	4	•
	DEC										7A	6	3	6A	7	2				M – 1 → M	•	•	↕	↕	4	•
Decrement stack pointer	DES	34	4	1																SP – 1 → SP	•	•	•	•	•	•
Decrement index register	DEX	09	4	1																X – 1 → X	•	•	•	↕	•	•
Complement (1's)	COMA	43	2	1																$\overline{A}$ → A	•	•	↕	↕	R	S
	COMB	53	2	1																$\overline{B}$ → B	•	•	↕	↕	R	S
	COM										73	6	3	63	7	2				$\overline{M}$ → M	•	•	↕	↕	R	S
Complement (2's)	NEGA	40	2	1																00 – A → A	•	•	↕	↕	1	2
	NEGB	50	2	1																00 – B → B	•	•	↕	↕	1	2
	NEG										70	6	3	60	7	2				00 – M → M	•	•	↕	↕	1	2
Decimal adjust accumulator	DAA	19	2	1																	•	•	↕	↕	↕	3

OP = Operation Code MC = Number of MPU Cycles PB = Number of Program Bytes

Instruction	Mnemonic	Addressing Mode: Implied			Immediate			Direct			Extended			Indexed			Relative			Boolean/Arith Operation	Condition Reg 5	4	3	2	1	0
		OP	MC	PB	OP	MC	PB	OP	MC	PB	OP	MC	PB	OP	MC	PB	OP	MC	PB		H	I	N	Z	V	C
Logical and	ANDA				84	2	2	94	3	2	B4	4	3	A4	5	2				A ● M → A	●	●	↕	↕	R	●
	ANDB				C4	2	2	D4	3	2	F4	4	3	E4	5	2				B ● M → B	●	●	↕	↕	R	●
Inclusive or	ORAA				8A	2	2	9A	3	2	BA	4	3	AA	5	2				A + M → A	●	●	↕	↕	R	●
	ORAB				CA	2	2	DA	3	2	FA	4	3	EA	5	2				B + M → B	●	●	↕	↕	R	●
Exclusive or	EORA				88	2	2	98	3	2	B8	4	3	A8	5	2				A ⊕ M → A	●	●	↕	↕	R	●
	EORB				C8	2	2	D8	3	2	F8	4	3	E8	5	2				B ⊕ M → B	●	●	↕	↕	R	●
Shift left arithmetic	ASLA	48	2	1																	●	●	↕	↕	6	↕
	ASLB	58	2	1																	●	●	↕	↕	6	↕
	ASL										78	6	3	68	7	2					●	●	↕	↕	6	↕
Shift right arithmetic	ASRA	47	2	1																	●	●	↕	↕	6	↕
	ASRB	57	2	1																	●	●	↕	↕	6	↕
	ASR										77	6	3	67	7	2					●	●	↕	↕	6	↕
Shift right logical	LSRA	44	2	1																	●	●	R	↕	6	↕
	LSRB	54	2	1																	●	●	R	↕	6	↕
	LSR										74	6	3	64	7	2					●	●	R	↕	6	↕
Rotate left	ROLA	49	2	1																	●	●	↕	↕	6	↕
	ROLB	59	2	1																	●	●	↕	↕	6	↕
	ROL										79	6	3	69	7	2					●	●	↕	↕	6	↕
Rotate right	RORA	46	2	1																	●	●	↕	↕	6	↕
	RORB	56	2	1																	●	●	↕	↕	6	↕
	ROR										76	6	3	66	7	2					●	●	↕	↕	6	↕
Compare accumulators	CBA	11	2	1																A – B	●	●	↕	↕	↕	↕
Compare	CMPA				81	2	2	91	3	2	B1	4	3	A1	5	2				A – M	●	●	↕	↕	↕	↕
	CMPB				C1	2	2	D1	3	2	F1	4	3	E1	5	2				B – M	●	●	↕	↕	↕	↕
Compare index register	CPX				8C	3	3	9C	4	2	BC	5	3	AC	6	2				X_H – M, X_L – (M+1)	●	●	7	↕	8	●
Test (zero or minus)	TSTA	4D	2	1																A – 00	●	●	↕	↕	R	R
	TSTB	5D	2	1																B – 00	●	●	↕	↕	R	R
	TST										7D	6	3	6D	7	2				M – 00	●	●	↕	↕	R	R
Bit test	BITA				85	2	2	95	3	2	B5	4	3	A5	5	2				A ● M	●	●	↕	↕	R	●
	BITB				C5	2	2	D5	3	2	F5	4	3	E5	5	2				B ● M TEST	●	●	↕	↕	R	●
Branch	BRA																20	4	2		●	●	●	●	●	●
Branch if carry clear	BCC																24	4	2	C = 0	●	●	●	●	●	●
Branch if carry set	BCS																25	4	2	C = 1	●	●	●	●	●	●
Branch if overflow clear	BVC																28	4	2	V = 0	●	●	●	●	●	●
Branch if overflow set	BVS																29	4	2	V = 1	●	●	●	●	●	●
Branch if equal to zero	BEQ																27	4	2	Z = 1	●	●	●	●	●	●
Branch if greater or equal to zero	BGE																2C	4	2	N ⊕ V = 0	●	●	●	●	●	●
Branch if greater than zero	BGT																2E	4	2	Z + (N ⊕ V) = 0	●	●	●	●	●	●
Branch if less than zero	BLT																2D	4	2	N ⊕ V = 1	●	●	●	●	●	●
Branch if less than or equal to zero	BLE																2F	4	2	Z + (N ⊕ V) = 1	●	●	●	●	●	●
Branch if not equal to zero	BNE																26	4	2	Z = 0	●	●	●	●	●	●
Branch if minus	BMI																2B	4	2	N = 1	●	●	●	●	●	●
Branch if plus	BPL																2A	4	2	N = 0	●	●	●	●	●	●
Branch if higher	BHI																22	4	2	C + Z = 0	●	●	●	●	●	●
Branch if lower or same	BLS																23	4	2	C + Z = 1	●	●	●	●	●	●

OP = Operation Code   MC = Number of MPU Cycles   PB = Number of Program Bytes

Instruction	Mnemonic	Implied			Direct			Immediate			Extended			Indexed			Relative			Boolean/Arith Operation	5 H	4 I	3 N	2 Z	1 V	0 C
		OP	MC	PB	OP	MC	PB	OP	MC	PB	OP	MC	PB	OP	MC	PB	OP	MC	PB							
Branch to subroutine	BSR																8D	8	2	See Special Operations	•	•	•	•	•	•
Jump to subroutine	JSR										BD	9	3	AD	8	2					•	•	•	•	•	•
Jump	JMP										7E	3	3	6E	4	2					•	•	•	•	•	•
Return from subroutine	RTS	39	5	1																	•	•	•	•	•	•
Return from interrupt	RTI	3B	10	1																	Note 10					
Software interrupt	SWI	3F	12	1																	•	S	•	•	•	•
Wait for interrupt	WAI	3E	9	1																	•	11	•	•	•	•
No operation	NOP	02	2	1																PC + 1 → PC	•	•	•	•	•	•
Clear	CLRA	4F	2	1																00 → A	•	•	R	S	R	R
	CLRB	5F	2	1																00 → B	•	•	R	S	R	R
	CLR										7F	6	3	6F	7	2				00 → M	•	•	R	S	R	R
Clear carry	CLC	0C	2	1																0 → C	•	•	•	•	•	R
Clear interrupt mask	CLI	0E	2	1																0 → I	•	R	•	•	•	•
Clear overflow	CLV	0A	2	1																0 → V	•	•	•	•	R	•
Set carry	SEC	0D	2	1																1 → C	•	•	•	•	•	S
Set interrupt mask	SEI	0F	2	1																1 → I	•	S	•	•	•	•
Set overflow	SEV	0B	2	1																1 → V	•	•	•	•	S	•

(Addressing Modes: Implied, Direct, Immediate, Extended, Indexed, Relative; Condition Reg.: bits 5–0 = H, I, N, Z, V, C)

CONDITION CODE SYMBOLS:

- H Half-carry from bit 3;
- I Interrupt mask
- N Negative (sign bit)
- Z Zero (byte)
- V Overflow, 2's complement
- C Carry from bit 7
- R Reset Always
- S Set Always
- ↕ Test and set if true, cleared otherwise
- • Not Affected

LEGEND:

- OP Operation Code (Hexadecimal);
- MC Number of MPU Cycles;
- PB Number of Program Bytes;
- + Arithmetic Plus;
- − Arithmetic Minus;
- • Boolean AND;
- M_{SP} Contents of memory location pointed to by Stack Pointer;
- + Boolean Inclusive OR;
- ⊕ Boolean Exclusive OR;
- $\overline{M}$ Complement of M;
- → Transfer Into;
- 0 Bit = Zero;
- 00 Byte = Zero;

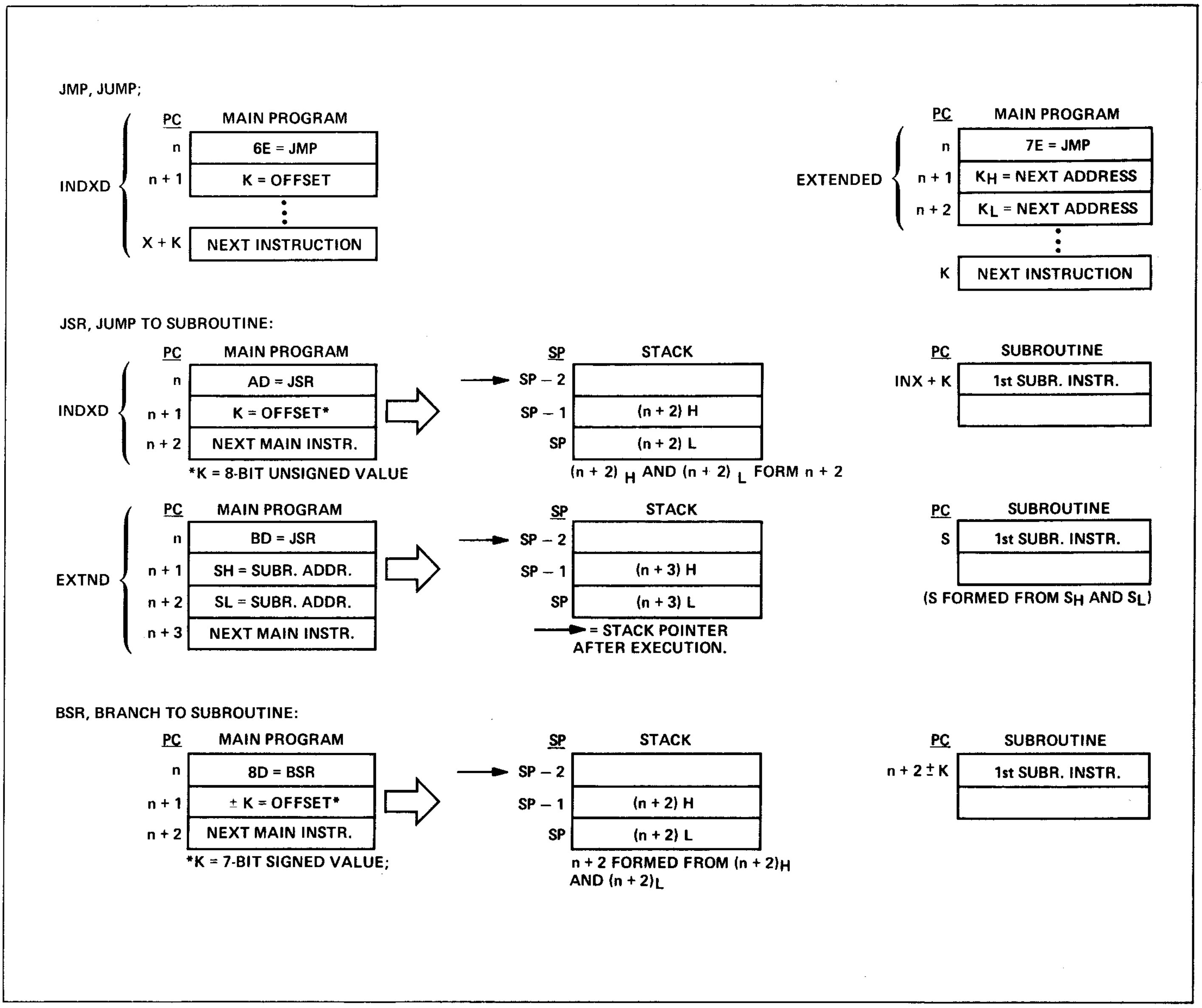
Note – Accumulator addressing mode instructions are included in the IMPLIED addressing.

CONDITION CODE REGISTER NOTES:

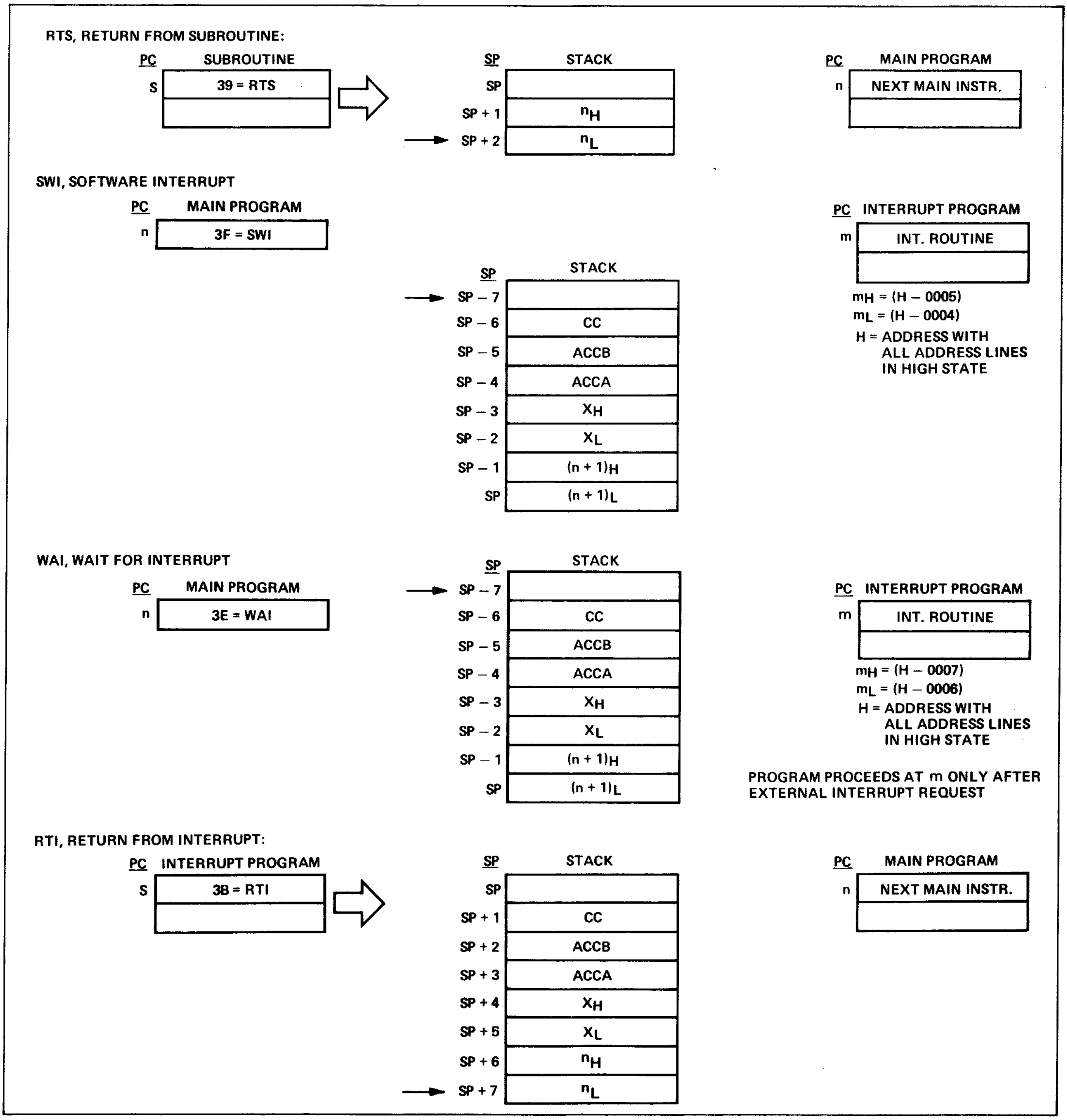
(Bit set if test is true and cleared otherwise)

1 (Bit V) Test: Result = 10000000?
2 (Bit C) Test: Result = 00000000?
3 (Bit C) Test: Decimal value of most significant BCD Character greater than nine? (Not cleared if previously set.)
4 (Bit V) Test: Operand = 10000000 prior to execution?
5 (Bit V) Test: Operand = 01111111 prior to execution?
6 (Bit V) Test: Set equal to result of N ⊕ C after shift has occurred.
7 (Bit N) Test: Sign bit of most significant (MS) byte = 1?
8 (Bit V) Test: 2's complement overflow from subtraction of MS bytes?
9 (Bit N) Test: Result less than zero? (Bit 15 = 1)
10 (All) Load Condition Code Register from Stack. (See Special Operations)
11 (Bit I) Set when interrupt occurs, if previously set, a Non-Maskable Interrupt is required to exit the wait state.
12 (ALL) Set according to the contents of Accumulator A

SPECIAL OPERATIONS



SPECIAL OPERATIONS



SYSTEMS OPERATION

To demonstrate the great versatility of the functional building block concept, a typical system configuration is shown. This configuration will demonstrate how easily a basic system may be upgraded and expanded for a number of different applications.

The Microprocessing Unit (MPU) may be configured with a Read Only Memory (ROM), Random Access Memory (RAM), a Peripheral Interface Adapter (PIA), restart circuitry and clock circuitry to form a minimum functional system (Figure 10). Such a system can easily be adapted for a number of small scale applications by simply changing the content of the ROM.

TWO-PHASE CLOCK CIRCUITRY AND TIMING–The MPU requires a two-phase non-overlapping clock which has a frequency range as high as 1 MHz. In addition to the two phases, this circuit should also generate an enable signal E, and its complement $\overline{E}$, to enable ROMs, RAMs, PIAs and ACIAs. This Enable signal and its complement is obtained by ANDing $\phi 2$ and VMA (Valid Memory Address).

CHIP SELECTION AND ADDRESSING–The minimum system configuration permits direct selection of the ROM, RAM, ACIA and PIA without the use of special TTL select logic. This is accomplished by simply wiring the address lines A13 and A14 to the Enable or chip select lines on the memories and PIA. This permits the devices to be addressed as follows:

Device	A14	A13	Hex Addresses
RAM	0	0	0000–007F
PIA	0	1	2004–2007 (Registers)
ROM	1	1	6000–63FF

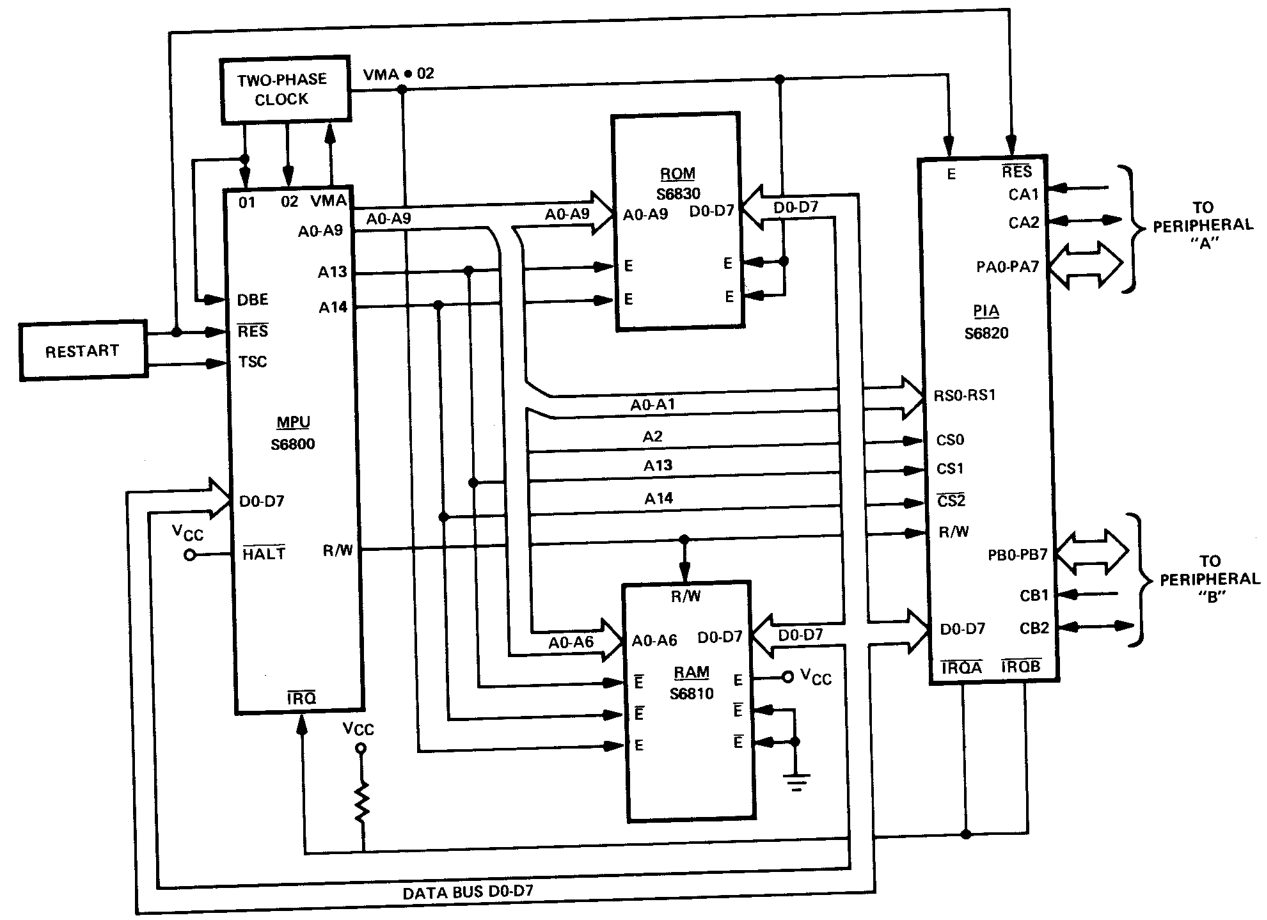
Other addressing schemes can be utilized which use any combination of two of the lines A10 through A14 for chip selection.

PERIPHERAL CONTROL–All control and timing for the peripherals that are connected to the PIA is accomplished by software routines under the control of the MPU.

RESTART AND NON-MASKABLE INTERRUPT–Since this basic system does not have a nonvolatile RAM, special circuitry to handle loss of power using NMI is not required. Circuitry is, however, required to insure proper initialization of the MPU when power is turned on. This circuit should insure that the Restart signal is held low for eight $\phi 1$ clock cycles after the V_{CC} power supply reaches a voltage of approximately 4.75 volts DC. Also, in order to insure that a PIA or ACIA is not inadvertently selected during the power-on sequence, Three-State Control (TSC) should be held high until the positive transition of Restart.

$\overline{\text{HALT}}$–The $\overline{\text{Halt}}$ line is tied to V_{CC} and will automatically place the MPU in the run state when power is turned on. This signal may be used to halt the MPU if a switch is used to tie the line to ground for HALT and to V_{CC} for RUN.

FIGURE 10 – MINIMUM SYSTEM CONFIGURATION

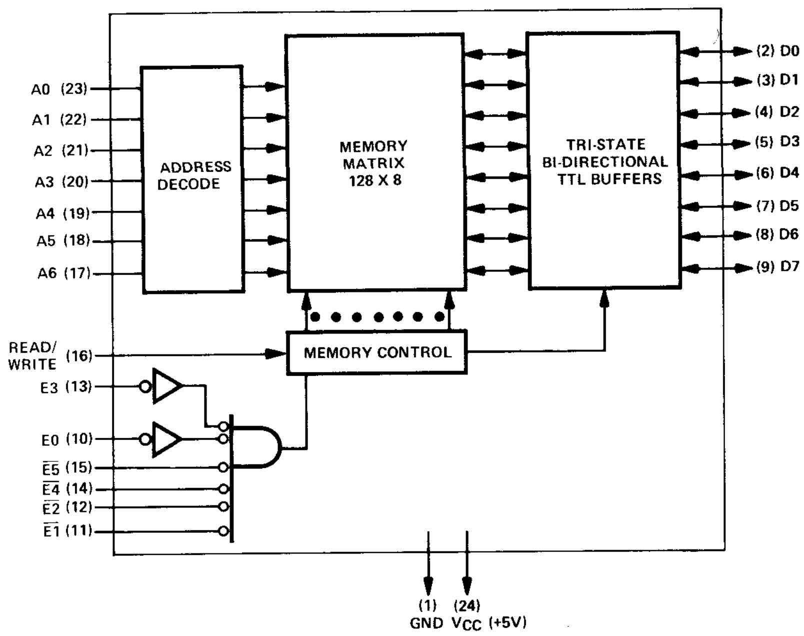


S6810

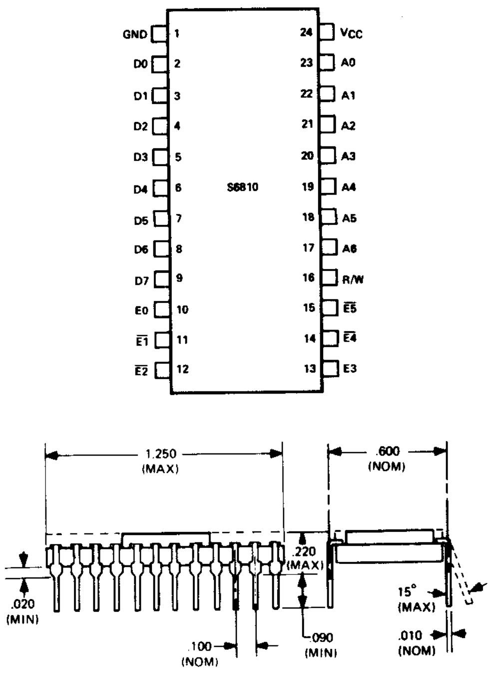
128 X 8 STATIC
READ/WRITE MEMORY

AMI
AMERICAN MICROSYSTEMS, INC.

ADVANCED PRODUCT DESCRIPTION



BLOCK DIAGRAM



PIN/PACKAGE CONFIGURATION

FEATURES

- Organized as 128 Bytes of 8 Bits
- Static Operation
- Bi-Directional Three-State Data Input/Output
- Six Chip Enable Inputs (Four Active Low, Two Active High)
- Single 5-Volt Power Supply
- TTL Compatible
- Maximum Access Time = 1.0μs for S6810
  575 ns for S6810-1

FUNCTIONAL DESCRIPTION

The S6810 is a static 128 x 8 Read/Write Memory designed and organized to be compatible with the S6800 Microprocessor. Interfacing to the S6810 consists of an 8 Bit Bi-directional Data Bus, Seven Address Lines, a single Read/Write Control line, and six Chip Enable lines, four negative and two positive.

For ease of use, the S6810 is a totally static memory requiring no clocks or cell refresh. The S6810 is fabricated with N channel silicon gate technology to be fully DTL/TTL compatible with only a single +5 volt power supply required.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage V_{CC}	-0.3 to +7.0V
Input Voltage V_{in}	-0.3 to +7.0V
Operating Temperature Range T_A	0 to +70°C
Storage Temperature Range T_{stg}	-55 to +150°C

DC (STATIC) CHARACTERISTICS

(V_{CC} = 5.0 Volt ± 5%; T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min.	Typ.	Max.	Unit	Condition
Input High Voltage (Normal Operating Levels)	V_{IH}	2.4	–	5.25	V	
Input Low Voltage (Normal Operating Levels)	V_{IL}	-0.3	–	0.4	V	
Input Current (A_n, R/W, E_n, $\overline{E}_n$) (V_{in} = 0 to 5.25 V)	I_{in}	–	–	2.5	μA	
Input High Threshold Voltage	V_{IHT}	2.0	–	–	V	
Input Low Threshold Voltage	V_{ILT}	–	–	0.8	V	
Output High Voltage (I_{OH} = −100 μA)	V_{OH}	2.4	–	–	V	
Output Low Voltage (I_{OL} = 1.6 mA)	V_{OL}	–	–	0.4	V	
Output Leakage Current (D0 – D7) (V_O = 2.4 V, E = 0.4 V, $\overline{E}$ = 2.4 V)	I_{LIH}	–	–	10	μA	
Output Leakage Current (D0 – D7) (V_O = 0.4 V, E = 0.4 V, $\overline{E}$ = 2.4 V)	I_{LOL}	–	–	10	μA	
Supply Current (V_{CC} = 5.25 V, T_A = 0°C)	I_{CC}	–	–	130	mA	
Input Capacitance	C_{IN}	–	–	7.5	pF	f = 1.0MHz, T_A = 25°C
Output Capacitance	C_{OUT}	–	–	15	pF	

AC (DYNAMIC) CHARACTERISTICS

(V_{CC} = 5.0 Volt ∓ 5%, T_A = 0°C to + 70°C)

Characteristic		Symbol	Min.	Max.	Unit
Address Setup Time		t_{AS}	30	–	ns
Address Hold Time		t_{AH}	0	–	ns
Chip Enable Pulse Width	S6810 S6810-1	t_{CS}	800 400	–	ns

READ CYCLE
(All timing with $t_r = t_f = 20$ ns, Load of Figure 1)

Characteristic		Symbol	Min.	Max.	Unit
Read Cycle Time	S6810 S6810-1	$t_{cyc(R)}$	1000 575	– –	ns ns
Output Enable Delay Time	S6810 S6810-1	t_{ED}	– –	400 300	ns ns
Output Disable Delay Time	S6810 S6810-1	t_{DD}	10 10	200 150	ns ns
Read Access Time	S6810 S6810-1	t_{acc}	– –	1000 575	ns ns

WRITE CYCLE
(All timing with $t_r = t_f = 20$ ns, Load of Figure 1)

Characteristic		Symbol	Min.	Max.	Unit
Write Cycle Time	S6810 S6810-1	$t_{cyc(W)}$	1000 500	– –	ns ns
Write Pulse Width	S6810 S6810-1	t_{WP}	800 400	– –	ns ns
Write Pulse Hold Time	S6810 S6810-1	t_{WH}	1000 500	– –	ns ns
Data Setup Time	S6810 S6810-1	t_{DS}	500 300	– –	ns ns
Data Hold Time	S6810 S6810-1	t_{DH}	0	–	ns

TIMING CHARACTERISTICS

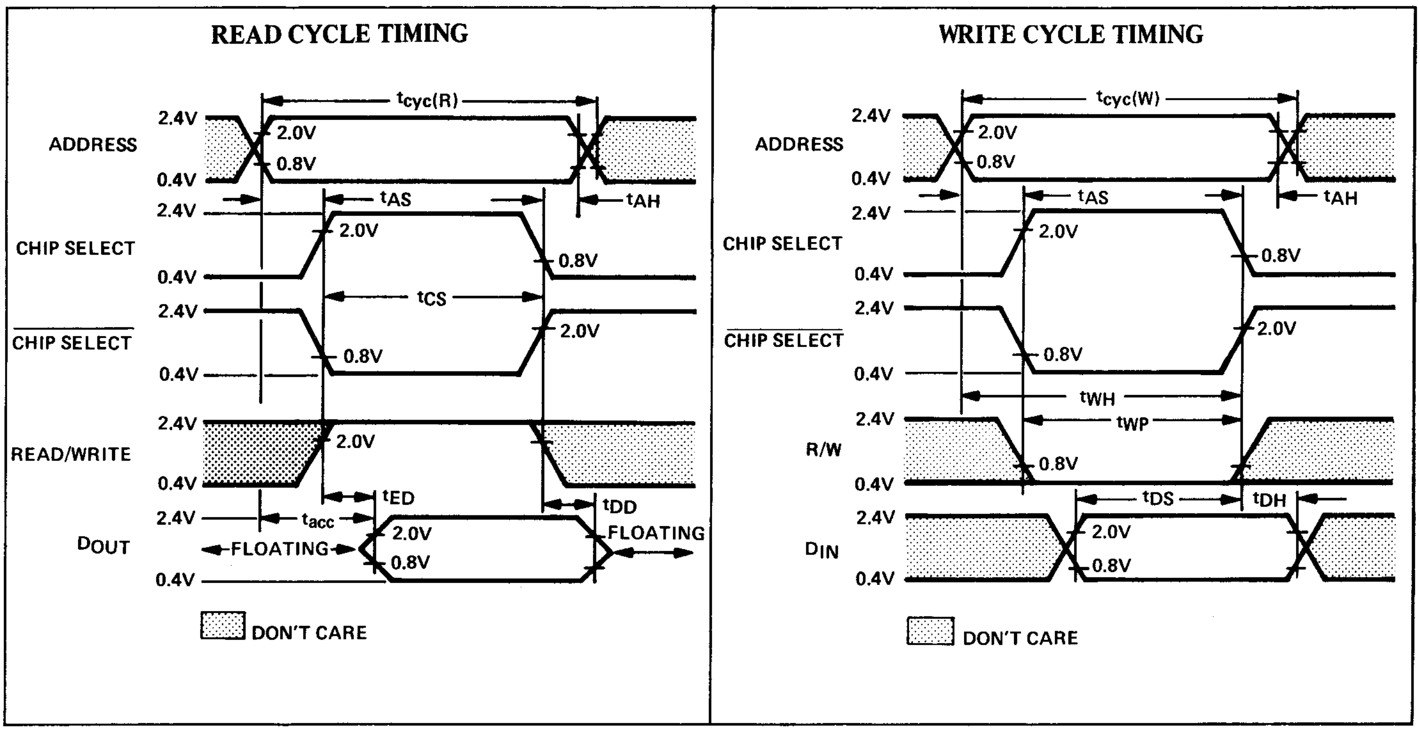
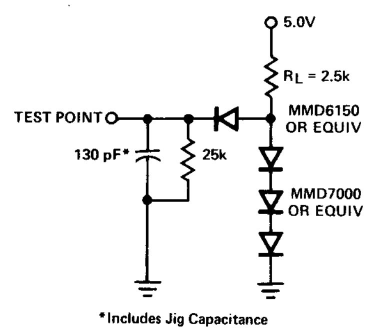


FIGURE 1 – AC TEST LOAD



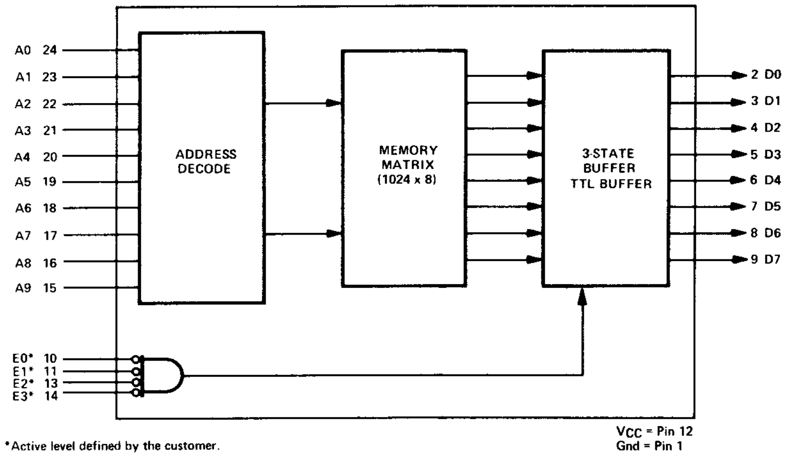
AMI
AMERICAN MICROSYSTEMS, INC.
3800 Homestead Road, Santa Clara, Ca. 95051/Telephone: (408) 246-0330, TWX: 910-338-0018

S6830

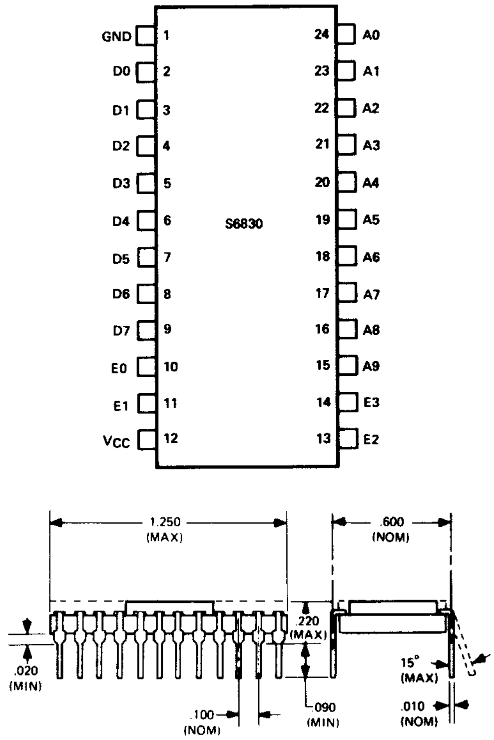
1024 X 8
READ ONLY MEMORY

AMI
AMERICAN MICROSYSTEMS, INC.

ADVANCED PRODUCT DESCRIPTION



BLOCK DIAGRAM



PIN/PACKAGE CONFIGURATION

FEATURES

- Organized as 1024-Bytes of 8 Bits
- Static Operation
- Three-State Data Output
- Four Chip Enable Inputs (Mask Programmable)
- Single 5-Volt Power Supply
- TTL Compatible Input/Output
- Maximum Access Time = 575 ns

FUNCTIONAL DESCRIPTION

The S6830 is a mask programmable read only memory organized 1024 words x 8 bits for application in byte organized systems. The S6830 is totally bus compatible with the S6800 microprocessor. Interfacing to the S6830 consists of an 8 bit three-state data bus, four mask programmable chip selects and ten address lines.

The S6830 is a totally static memory requiring no clocks. Access time is compatible with maximum data rates in a S6800 microprocessor system. The device operates from a single +5 volt power supply and is fabricated with N channel silicon gate technology.

ABSOLUTE MAXIMUM RATINGS (See Note 1)

Supply Voltage V_{CC}	-0.3 to +7.0V
Input Voltage V_{in}	-0.3 to +7.0V
Operating Temperature Range T_A	0 to +70°C
Storage Temperature Range T_{stg}	-55 to +150°C

NOTE: 1. Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

DC (STATIC) CHARACTERISTICS
(V_{CC} = +5 Volt ± 5%; T_A = 0°C to +70°C)

RECOMMENDED DC OPERATING CONDITIONS

Parameter	Symbol	Min.	Max.	Unit
Input High Voltage (Norm. Op. Levels)	V_{IH}	2.4	5.25	Vdc
Input Low Voltage (Norm. Op. Levels)	V_{IL}	-0.3	0.4	Vdc
Input Current (V_{in} = 0 to 5.25 V)	I_{in}	–	2.5	μAdc
Input High Threshold Voltage	V_{IHT}	2.0	–	Vdc
Input Low Threshold Voltage	V_{ILT}	–	0.65	Vdc
Output High Voltage (I_{OH} = -100 μA)	V_{OH}	2.4	–	Vdc
Output Low Voltage (I_{OL} = 1.6 mA)	V_{OL}	–	0.45	Vdc
Output Leakage Current (V_{OH} = 2.4 V, E = 0.4 V, $\overline{E}$ = 2.4 V)	I_{LOH}	–	10	μAdc
Output Leakage Current (V_{OH} = 0.4 V, E = 0.4 V, $\overline{E}$ = 2.4 V)	I_{LOL}	–	10	μAdc
Supply Current (V_{CC} @ 5.25V, T_A = 0°C)	I_{CC}	–	130	mAdc

CAPACITANCE

Characteristic	Symbol	Min.	Typ.	Max.	Unit	Conditions
Input Capacitance	C_{in}	–	–	7.5	pF	f = 1.0 MHz
Output Capacitance	C_{out}	–	–	15	pF	T_A = 25°C

AC (DYNAMIC) CHARACTERISTICS

V_{CC} = +5 Volt ± 5%; T_A = 0°C to +70°C

READ CYCLE (All timing with $t_r = t_f$ = 20 ns, Load of Figure 1)

Characteristic	Symbol	Min.	Max.	Unit
Read Cycle Time	t_{cyc} (R)	575	–	ns
Output Enable Delay Time	t_{ED}	–	300	ns
Output Disable Delay Time	t_{DD}	10	150	ns
Read Access Time	t_{acc}	–	575	ns

READ CYCLE TIMING

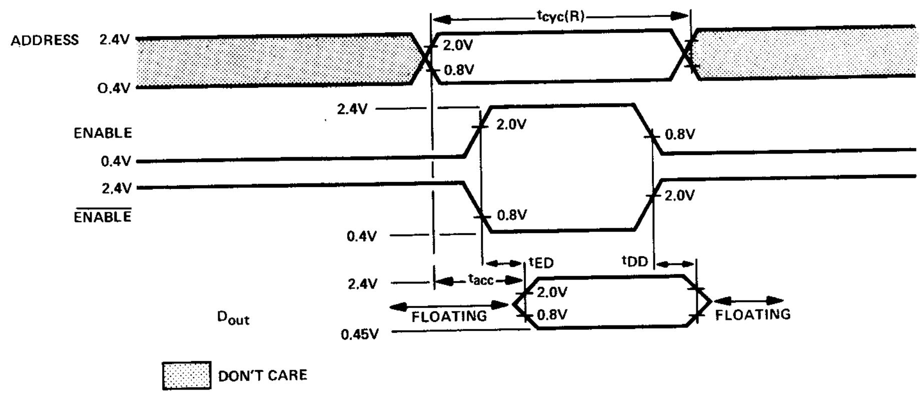
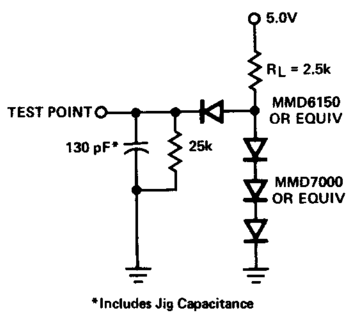


FIGURE 1 – AC TEST LOAD



CUSTOM PROGRAMMING

Programming the S6830 is most accurately and economically accomplished by submitting a deck of 36 punched cards to AMI. On these cards the contents of memory and chip enable inputs are to be specified.

The first card is an identification card, the following 34 cards are data cards, and the final card contains the chip enable code. Card format is as follows:

First Card

Col. 1 – 11	Product Name (1K x 8 NROM)
12 – 19	Blank
20 – 60	Customer Name
61 – 72	Blank
73 – 75	Customer ID – number assigned by AMI marketing
76	Hyphen
77 – 78	Card number (01) in decimal
79 – 80	Total number of cards (36) in decimal

Card 2

Col. 1 – 11	Blank
12	Hexidecimal equivalent for MS (most significant) Character of byte "O" of program
13	Hexidecimal equivalent for LS Character of byte "O" of program

Example: If binary character is 1011 0010, the most significant bits (1011 or "B") is punched into column 12 and the least significant bits (0010 or "2") is punched into column 13.

Col. 14 – 15	Hex equivalent for byte "1"
16 – 73	Hex equivalent for each successive byte in the program
74 – 76	Blank.
77 – 78	Card sequence number. (02) in decimal

Cards 3 through 35

Continue through the entire program as described for card 2.

Card 36

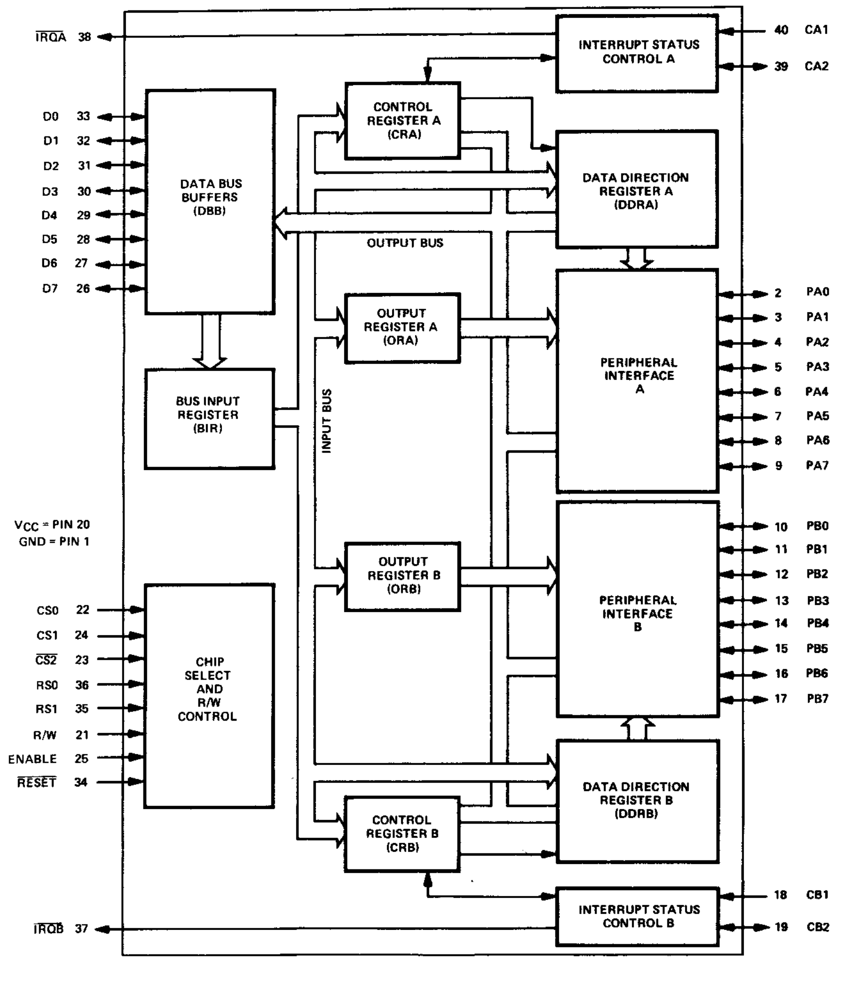
Col. 1 – 11	Blank
12	E3 Chip Enable Code (1 = True, 0 = False)
13	E2
14	E1
15	E0
16 – 76	Blank
77 – 78	Card sequence number (36) in decimal

S6820

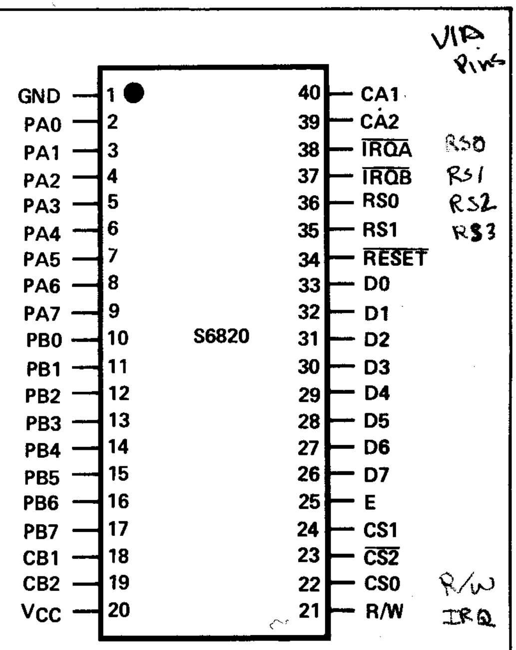
PERIPHERAL INTERFACE
ADAPTER (PIA)

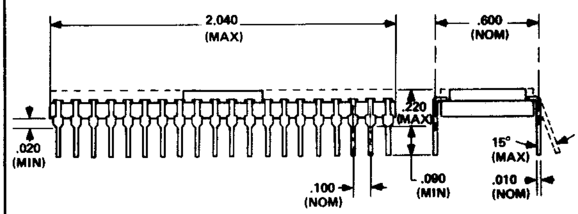
AMI
AMERICAN MICROSYSTEMS, INC.

ADVANCED PRODUCT DESCRIPTION



BLOCK DIAGRAM





PIN/PACKAGE CONFIGURATION

FEATURES

- 8-Bit Bidirectional Data Bus for Communication with the MPU
- Two Bidirectional 8-Bit Buses for Interface to Peripherals
- Two Programmable Control Registers
- Two Programmable Data Direction Registers
- Four Individually-Controlled Interrupt Input Lines; Two Usable as Peripheral Control Outputs
- Handshake Control Logic for Input and Output Peripheral Operation
- High-Impedance 3-State and Direct Transistor Drive Peripheral Lines
- Program Controlled Interrupt and Interrupt Disable Capability
- CMOS Compatible Peripheral Lines

FUNCTIONAL DESCRIPTION

The S6820 Peripheral Interface Adapter provides the universal means of interfacing peripheral equipment to the S6800 Microprocessing Unit (MPU). This device is capable of interfacing the MPU to peripherals through two 8-bit bidirectional peripheral data buses and four control lines. No external logic is required for interfacing to most peripheral devices.

The functional configuration of the PIA is programmed by the MPU during system initialization. Each of the peripheral data lines can be programmed to act as an input or output, and each of the four control/interrupt lines may be programmed for one of several control modes. This allows a high degree of flexibility in the over-all operation of the interface.

The PIA interfaces to the S6800 MPU with an eight-bit bidirectional data bus, three chip select lines, two register select lines, two interrupt request lines, read/write line, enable line and reset line. These signals, in conjunction with the S6800 VMA output, permit the MPU to have complete control over the PIA. VMA may be utilized to gate the input signals to the PIA.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage V_{CC}	–0.3 to +7.0V
Input Voltage V_{in}	–0.3 to +7.0V
Operating Temperature Range T_A	0 to +70°C
Storage Temperature Range T_{stg}	–55 to +150°C

NOTE: This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields, however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

DC (STATIC) CHARACTERISTICS

(V_{CC} = 5.0V ± 5%, T_A = 25°C unless otherwise noted.)

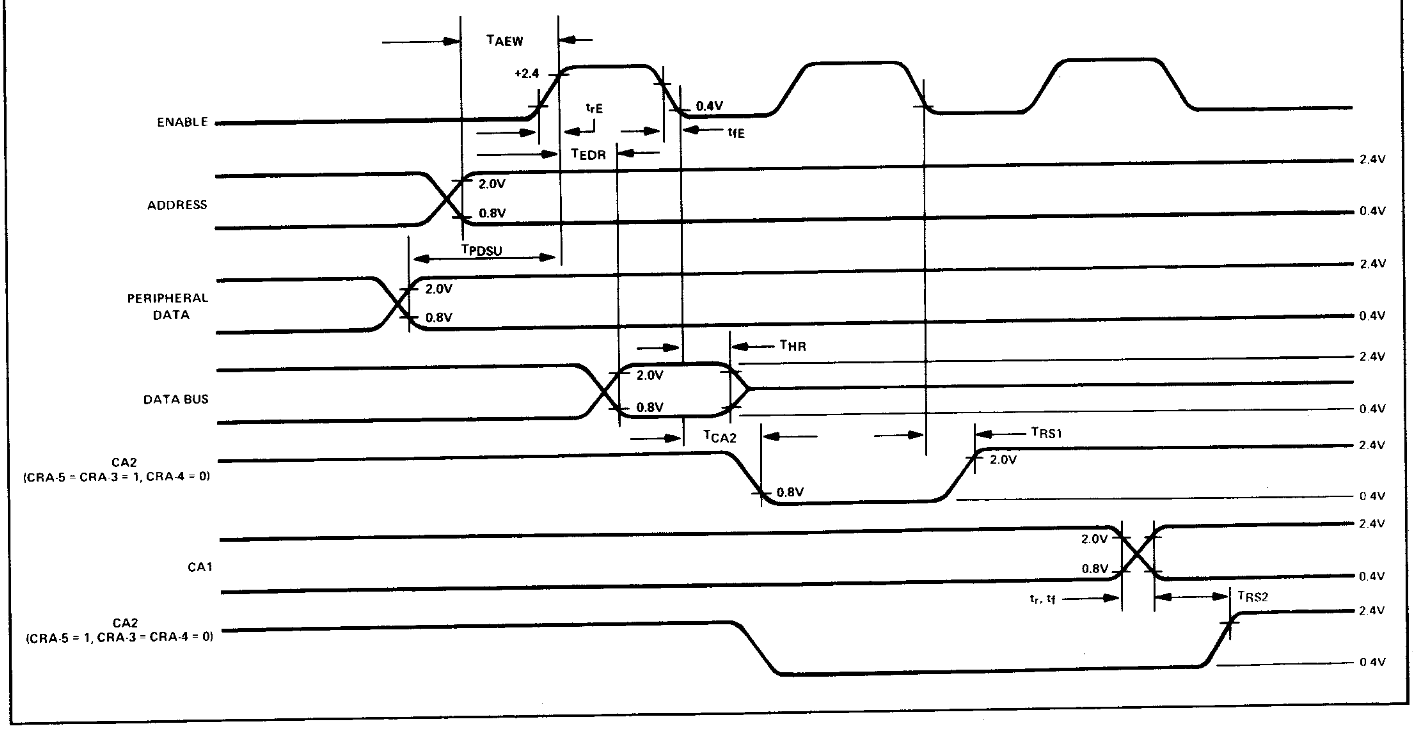
Characteristic	Symbol	Min.	Typ.	Max.	Unit
Input High Voltage (Normal Operating Levels)	V_{IH}	+2.4	–	V_{CC}	Vdc
Input Low Voltage (Normal Operating Levels)	V_{IL}	–0.3	–	+0.4	Vdc
Input High Threshold Voltage All Inputs Except Enable	V_{IHT}	+2.0	–	–	Vdc
Input Low Threshold Voltage All Inputs Except Enable	V_{ILT}	–	–	+0.8	Vdc
Input Leakage Current (V_{in} = 0 to 5.0 Vdc) R/W, $\overline{\text{Reset}}$, RS0, RS1, CS0, CS1, $\overline{\text{CS2}}$, CA1, CB1, Enable	I_{in}	–	1.0	2.5	μAdc
Three-State (Off State) Input Current (V_{in} = 0.4 to 2.4 Vdc, V_{CC} = max) D0-D7, PB0-PB7, CB2	I_{TSI}	–	2.0	10	μAdc
Input High Current PA0-PA7, CA2 (V_{IH} = 2.4 Vdc)	I_{IH}	100	250	–	μAdc
Input Low Current PA0-PA7, CA2 (V_{IL} = 0.4 Vdc)	I_{IL}	–	1.0	1.6	mAdc
Output High Voltage (V_{CC} = min, I_{Load} = –100 μAdc, Enable Pulse Width < 25 μs)	V_{OH}	+2.4	–	–	Vdc
Output Low Voltage (V_{CC} = min, I_{Load} = 1.6 mAdc)	V_{OL}	–	–	+0.4	Vdc
Output High Current (Sourcing) (V_{OH} = 2.4 Vdc) (V_{OH} = 1.5 Vdc, the current for driving other than TTL, e.g., Darlington Base) PB0-PB7, CB2	I_{OH}	–100 –1.0	–1000 –2.5	– –	μAdc mAdc
Output Low Current (Sinking) (V_{OL} = 0.4 Vdc)	I_{OL}	1.6	–	–	mAdc
Output Leakage Current (Off State) $\overline{\text{IRQA}}$, $\overline{\text{IRQB}}$	I_{off}	–	1.0	10	μAdc
Power Dissipation	P_D	–	300	600	mW
Input Capacitance (V_{in} = 0, T_A = 25°C, f = 1.0 MHz) D0-D7, PA0-PA7, PB0-PB7, CA2, CB2 R/W, $\overline{\text{Reset}}$, RS0, RS1, CS0, CS1, $\overline{\text{CS2}}$, CA1, CB1 Enable	C_{in}	– – –	– – –	10 7.0 20	pF
Output Capacitance (V_{in} = 0, T_A = 25°C, f = 1.0 MHz)	C_{out}	–	–	10	pF

AC (DYNAMIC) CHARACTERISTICS Loading = 30 pF and one TTL load for PA0-PA7, PB0-PB7, CA2, CB2
= 130 pF and one TTL load for D0-D7, $\overline{IRQA}$, $\overline{IRQB}$

READ TIMING CHARACTERISTICS (Figure 1)

Characteristic	Symbol	Min.	Typ.	Max.	Unit
Delay Time, Address valid to Enable positive transition	T_{AEW}	180	–	–	ns
Delay Time, Enable positive transition to Data valid on bus	T_{EDR}	–	–	395	ns
Peripheral Data Setup Time	T_{PDSU}	300	–	–	ns
Data Bus Hold Time	T_{HR}	10	–	–	ns
Delay Time, Enable negative transition to CA2 negative transition	T_{CA2}	–	–	1.0	μs
Delay Time, Enable negative transition to CA2 positive transition	T_{RS1}	–	–	1.0	μs
Rise and Fall Time for CA1 and CA2 input signals	t_r, t_f	–	–	1.0	μs
Delay Time from CA1 active transition to CA2 positive transition	T_{RS2}	–	–	2.0	μs
Rise and Fall Time for Enable input	t_{rE}, t_{fE}	–	–	25	μs

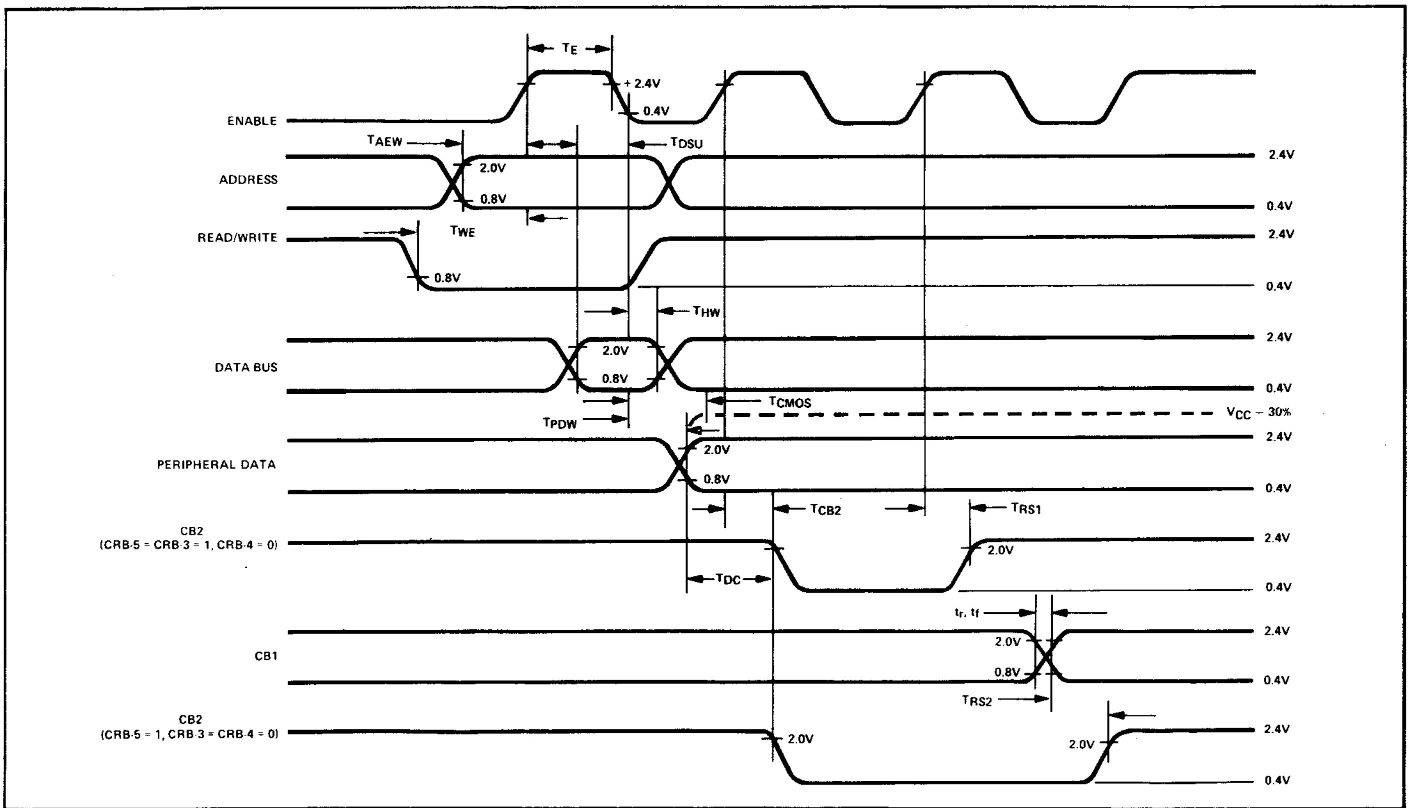
FIGURE 1 – READ TIMING CHARACTERISTICS



WRITE TIMING CHARACTERISTICS (Figure 2)

Characteristic	Symbol	Min.	Typ.	Max.	Unit
Enable Pulse Width	T_E	0.470	–	25	μs
Delay Time, Address valid to Enable positive transition	T_{AEW}	180	–	–	ns
Delay Time, Data valid to Enable negative transition	T_{DSU}	300	–	–	ns
Delay Time, Read/Write negative transition to Enable positive transition	T_{WE}	130	–	–	ns
Data Bus Hold Time.	T_{HW}	10	–	–	ns
Delay Time, Enable negative transition to Peripheral Data valid	T_{PDW}	–	–	1.0	μs
Delay Time, Enable negative transition to Peripheral Data valid, CMOS (V_{CC} - 30%) PA0-PA7, CA2	T_{CMOS}	–	–	2.0	μs
Delay Time, Enable positive transition to CB2 negative transition	T_{CB2}	–	–	1.0	μs
Delay Time, Peripheral Data valid to CB2 negative transition	T_{DC}	0	–	1.5	μs
Delay Time, Enable positive transition to CB2 positive transition	T_{RS1}	–	–	1.0	μs
Rise and Fall Time for CB1 and CB2 input signals	t_r, t_f	–	–	1.0	μs
Delay Time, CB1 active transition to CB2 positive transition	T_{RS2}	–	–	2.0	μs

FIGURE 2 – WRITE TIMING CHARACTERISTICS



INTERFACE DESCRIPTION

MPU/PIA INTERFACE

Pin	Label	Function
(33) (32) (31) (30) (29) (28) (27) (26)	D0 D1 D2 D3 D4 D5 D6 D7	**Bi-Directional Data** – The bi-directional data lines (D0-D7) allow the transfer of data between the MPU and the PIA. The data bus output drivers are three-state devices that remain in the high-impedance (off) state except when the MPU performs a PIA read operation. The Read/Write line is in the Read (high) state when the PIA is selected for a Read operation.
(25)	E	**Enable** – The enable pulse, E, is the only timing signal that is supplied to the PIA. Timing of all other signals is referenced to the leading and trailing edges of the E pulse. This signal will normally be a derivative of the S6800 $\phi 2$ Clock. The E pulse is used to condition the interrupt/control lines CA1, CA2, CB1, and CB2. At least one E pulse must occur from the inactive edge to the active edge of the input signal to set the interrupt flag, when the lines are used as inputs.
(21)	R/W	**Read/Write** – This signal is generated by the MPU to control the direction of data transfers on the Data Bus. A low state on the PIA Read/Write line enables the input buffers and data is transferred from the MPU to the PIA on the E signal if the device has been selected. A high on the Read/Write line sets up the PIA for a transfer of data to the bus. The PIA output buffers are enabled when the proper address and the enable pulse E are present.
(34)	$\overline{\text{RESET}}$	**$\overline{\text{Reset}}$** – The active low $\overline{\text{Reset}}$ line is used to reset all register bits in the PIA to a logical zero (low). This line can be used as a power-on reset and as a master reset during system operation.
(22) (24) (23)	CS0 CS1 $\overline{\text{CS2}}$	**Chip Select** – These three input signals are used to select the PIA. CS0 and CS1 must be high and $\overline{\text{CS2}}$ must be low for selection of the device. Data transfers are then performed under the control of the Enable and Read/Write signals. The chip select lines must be stable for the duration of the E pulse.
(36) (35)	RS0 RS1	**PIA Register Select** – The two register select lines are used to select the various registers inside the PIA. These two lines are used in conjunction with internal Control Registers to select a particular register that is to be written or read. The Register select lines should be stable for the duration of the E pulse while in the read or write cycle.

(38) (37)	$\overline{IRQA}$ $\overline{IRQB}$	**Interrupt Request** – The active low Interrupt Request lines ($\overline{IRQA}$ and $\overline{IRQB}$) act to interrupt the MPU either directly or through interrupt priority circuitry. These lines are "open source" (no load device on the chip) and are capable of sinking a current of 1.6 mA from an external source. This permits all interrupt request lines to be tied together in a wire-OR configuration. Each Interrupt Request line has two internal interrupt flag bits that will cause the Interrupt Request line to go low. Each flag bit is associated with a particular peripheral interrupt line. Also four interrupt enable bits are provided in the PIA which may be used to inhibit a particular interrupt from a peripheral device. Servicing an interrupt by the MPU is accomplished by a software routine that, on a prioritized basis, sequentially reads and tests the two control registers in each PIA for interrupt flag bits that are set. The Interrupt Flag is cleared (zeroed) as a result of an MPU Read Peripheral Data Operation.

PIA/PERIPHERAL INTERFACE

Pin	Label	Function
(2) (3) (4) (5) (6) (7) (8) (9)	PA0 PA1 PA2 PA3 PA4 PA5 PA6 PA7	**Section A Peripheral Data** – Each of the peripheral data lines can be programmed to act as an input or output. This is accomplished by setting a "1" in the corresponding Data Direction Register bit for those lines which are to be outputs. A "0" in a bit of the Data Direction Register causes the corresponding peripheral data line to act as an input. During an MPU Read Peripheral Data Operation, the data on peripheral lines programmed to act as inputs appears directly on the corresponding MPU Data Bus lines. In the input mode the internal pullup resistor on these lines represents a maximum of one standard TTL load. The data in Output Register A will appear on the data lines that are programmed to be outputs. A logical "1" written into the register will cause a "high" on the corresponding data line while a "0" results in a "low". Data in Output Register A may be read by an MPU "Read Peripheral Data A" operation when the corresponding lines are programmed as outputs. This data will be read properly if the voltage on the peripheral data lines is greater than 2.0 volts for a logic "1" output and less than 0.8 volt for a logic "0" output. Loading the output lines such that the voltage on these lines does not reach full voltage causes the data transferred into the MPU on a Read operation to differ from that contained in the respective bit of Output Register A.
(10) (11) (12) (13) (14) (15) (16) (17)	PB0 PB1 PB2 PB3 PB4 PB5 PB6 PB7	**Section B Peripheral Data** – The peripheral data lines in the B Section of the PIA can be programmed to act as either inputs or outputs in a similar manner to PA0-PA7. However, the output buffers driving these lines differ from those driving lines PA0-PA7. They have three-state capability, allowing them to enter a high impedance state when the peripheral data line is used as an input. In addition, data on the peripheral data lines PB0-PB7 will be read properly from those lines programmed as outputs even if the voltages are below 2.0 volts for a "high". As outputs, these lines are compatible with standard TTL and may also be used as a source of up to 1 milliampere at 1.5 volts to directly drive the base of a transistor switch.

Pin	Label	Function
(40) (18)	CA1 CB1	**Interrupt Input** – Peripheral Input lines CA1 and CB1 are input-only lines that set the interrupt flags of the control registers. The active transition for these signals is also programmed by the two control registers.
(39)	CA2	**Peripheral Control** – The peripheral control line CA2 can be programmed to act as an interrupt input or as a peripheral control output. As an output, this line is compatible with standard TTL; as an input the internal pullup resistor on this line represents one standard TTL load. The function of this signal line is programmed with Control Register A.
(19)	CB2	**Peripheral Control** – Peripheral Control line CB2 may also be programmed to act as an interrupt input or peripheral control output. As an input, this line has high input impedance and is compatible with standard TTL. As an output it is compatible with standard TTL and may also be used as a source of up to 1 milliampere at 1.5 volts to directly drive the base of a transistor switch. This line is programmed by Control Register B.
(1)	GND	**Ground**
(20)	V_{CC}	+5 Volts ± 5%

APPLICATION INFORMATION

INITIALIZATION

A low reset line has the effect of zeroing all PIA registers. This will set PA0-PA7, PB0-PB7, CA2 and CB2 as inputs, and all interrupts disabled. The PIA must be configured during the restart program which follows the reset.

REGISTER ADDRESSING

There are six locations within the PIA accessible to the MPU data bus; two Peripheral Registers, two Data Direction Registers, and two Control Registers, Selection of these locations is controlled by the RS0 and RS1 inputs together with bit 2 in the Control Register, as shown in Table 1.

TABLE 1 – INTERNAL ADDRESSING

RS1	RS0	Control Register Bit CRA-2	Control Register Bit CRB-2	Location Selected
0	0	1	X	Peripheral Register A
0	0	0	X	Data Direction Register A
0	1	X	X	Control Register A
1	0	X	1	Peripheral Register B
1	0	X	0	Data Direction Register B
1	1	X	X	Control Register B

X = Don't Care

DATA DIRECTION REGISTERS (DDRA and DDRB)

The two Data Direction Registers allow the MPU to control the direction of data through each corresponding peripheral data line. All Data Direction Register bits set at "0" configure the corresponding peripheral data line as an input; all "1s" result in an output.

CONTROL REGISTERS (CRA and CRB)

The two Control Registers (CRA and CRB) allow the MPU to control the operation of the four peripheral control lines CA1, CA2, CB1 and CB2. In addition they allow the MPU to enable the interrupt lines and monitor the status of the interrupt flags. Bits 0 through 5 of the two registers may be written or read by the MPU when the proper chip select and register select signals are applied. Bits 6 and 7 of the two registers are read only and are modified by external interrupts occurring on control lines CA1, CA2, CB1 or CB2. The format of the control words is shown in Table 2.

TABLE 2 – CONTROL WORD FORMAT

	7	6	5	4	3	2	1	0
CRA	IRQA1	IRQA2	CA2 Control			DDRA Access	CA1 Control	
	7	6	5	4	3	2	1	0
CRB	IRQB1	IRQB2	CB2 Control			DDRB Access	CB1 Control	

0 = data direction
1 = peripheral reg.

Data Direction Access Control Bit (CRA-2 and CRB-2) – Bit 2 in each Control register (CRA and CRB) allows selection of either a Peripheral Interface Register or the Data Direction Register when the proper register select signals are applied to RS0 and RS1.

Control of CA1 and CB1 Interrupt Input Lines (CRA-0, CRB-0, CRA-1, and CRB-1) – The two lowest order bits of the control registers are used to control the interrupt input lines CA1 and CB1. Bits CRA-0 and CRB-0 are used to enable the MPU interrupt signals $\overline{IRQA}$ and $\overline{IRQB}$, respectively. Bits CRA-1 and CRB-1 determine the active transition of the interrupt input signals CA1 and CB1 (Table 3).

TABLE 3 – CONTROL OF INTERRUPT INPUTS CA1 AND CB1

CRA-1 (CRB-1)	CRA-0 (CRB-0)	Interrupt Input CA1 (CB1)	Interrupt Flag CRA-7 (CRB-7)	MPU Interrupt Request $\overline{IRQA}$ $(\overline{IRQB})$
0	0	↓ Active	Set high on ↓ of CA1 (CB1)	Disabled – $\overline{IRQ}$ remains high
0	1	↓ Active	Set high on ↓ of CA1 (CB1)	Goes low when the interrupt flag bit CRA-7 (CRB-7) goes high
1	0	↑ Active	Set high on ↑ of CA1 (CB1)	Disabled – $\overline{IRQ}$ remains high
1	1	↑ Active	Set high on ↑ of CA1 (CB1)	Goes low when the interrupt flag bit CRA-7 (CRB-7) goes high

NOTES:
1. ↑ indicates positive transition (low to high)
2. ↓ indicates negative transition (high to low)
3. The Interrupt flag bit CRA-7 is cleared by an MPU Read of the A Data Register, and CRB-7 is cleared by an MPU Read of the B Data Register.
4. If CRA-0 (CRB-0) is low when an interrupt occurs (Interrupt disabled) and is later brought high, $\overline{IRQA}$ $(\overline{IRQB})$ occurs on the positive transition of CRA-0 (CRB-0).

Control of CA2 and CB2 Peripheral Control Lines (CRA-3, CRA-4, CRA-5, CRB-3, CRB-4, and CRB-5) – Bits 3, 4, and 5 of the two control registers are used to control the CA2 and CB2 Peripheral Control lines. These bits determine if the control lines will be an interrupt input or an output control signal. If bit CRA-5 (CRB-5) is low, CA2 (CB2) is an interrupt input line similar to CA1 (CB1) (Table 4). When CRA-5 (CRB-5) is high, CA2 (CB2) becomes an output signal that may be used to control peripheral data transfers. When in the output mode, CA2 and CB2 have slightly different characteristics (Tables 5 and 6).

TABLE 4 – CONTROL OF CA2 AND CB2 AS INTERRUPT INPUTS
CRA5 (CRB5) is low

CRA-5 (CRB-5)	CRA-4 (CRB-4)	CRA-3 (CRB-3)	Interrupt Input CA2 (CB2)	Interrupt Flag CRA-6 (CRB-6)	MPU Interrupt Request $\overline{IRQA}$ $(\overline{IRQB})$
0	0	0	↓ Active	Set high on ↓ of CA2 (CB2)	Disabled – $\overline{IRQ}$ remains high
0	0	1	↓ Active	Set high on ↓ of CA2 (CB2)	Goes low when the interrupt flag bit CRA-6 (CRB-6) goes high
0	1	0	↑ Active	Set high on ↑ of CA2 (CB2)	Disabled – $\overline{IRQ}$ remains high
0	1	1	↑ Active	Set high on ↑ of CA2 (CB2)	Goes low when the interrupt flag bit CRA-6 (CRB-6) goes high

NOTES:
1. ↑ indicates positive transition (low to high)
2. ↓ indicates negative transition (high to low)
3. The Interrupt flag bit CRA-6 is cleared by an MPU Read of the A Data Register and CRB-6 is cleared by an MPU Read of the B Data Register.
4. If CRA-3 (CRB-3) is low when an interrupt occurs (Interrupt disabled) and is later brought high, $\overline{IRQA}$ $(\overline{IRQB})$ occurs on the positive transition of CRA-3 (CRB-3).

TABLE 5 – CONTROL OF CA2 AS AN OUTPUT
CRA-5 is high

CRA-5	CRA-4	CRA-3	CA2 Cleared	CA2 Set
1	0	0	Low on negative transition of E after an MPU Read "A" Data operation.	High on an active transition of the CA1 signal
1	0	1	Low immediately after an MPU Read "A" Data operation.	High on the negative edge of the next "E" pulse.
1	1	0	Low when CRA-3 goes low as a result of an MPU Write in Control Register "A".	Always low as long as CRA-3 is low.
1	1	1	Always high as long as CRA-3 is high	High when CRA-3 goes high as a result of a Write in Control Register "A".

TABLE 6 – CONTROL OF CB2 AS AN OUTPUT
CRB-5 is high

CRB-5	CRB-4	CRB-3	CB2 Cleared	CB2 Set
1	0	0	Low on the positive transition of the first E pulse following an MPU Write "B" Data Register operation.	High when the interrupt flag bit CRB-7 is set by an active transition of the CB1 signal
1	0	1	Low on the positive transition of the first E pulse following an MPU Write "B" Data Register operation.	High on the positive transition of the next "E" pulse.
1	1	0	Low when CRB-3 goes low as a result of an MPU Write in Control Register "B".	Always low as long as CRB-3 is low. Will go high on an MPU Write in Control Register "B" that changes CRB-3 to "one".
1	1	1	Always high as long as CRB-3 is high. Will be cleared when an MPU Write Control Register "B" results in clearing CRB-3 to "zero".	High when CRB-3 goes high as a result of an MPU write into control register "B".

Interrupt Flags (CRA-6, CRA-7, CRB-6, and CRB-7) – The four interrupt flag bits are set by active transitions of signals on the four Interrupt and Peripheral Status lines when those lines are programmed to be interrupt inputs. These bits cannot be set directly from the MPU Data Bus and are reset indirectly by a Read Peripheral Data Operation on the appropriate section.

BASIC SYSTEM CONFIGURATION

The Microprocessing Unit (MPU) may be configured with a Read Only Memory (ROM), Random Access Memory (RAM), a Peripheral Interface Adapter (PIA), restart circuitry and clock circuitry to form a minimum functional system (Figure 3). Such a system can easily be adapted for a number of small scale applications by simply changing the content of the ROM.

TWO-PHASE CLOCK CIRCUITRY AND TIMING—The MPU requires a two-phase non-overlapping clock which has a frequency range as high as 1 MHz. In addition to the two phases, this circuit should also generate an enable Signal E, and its complement E, to enable ROMs, RAMs, PIAs and ACIAs. This Enable signal and its complement is obtained by ANDing ϕ2 and VMA (Valid Memory Address).

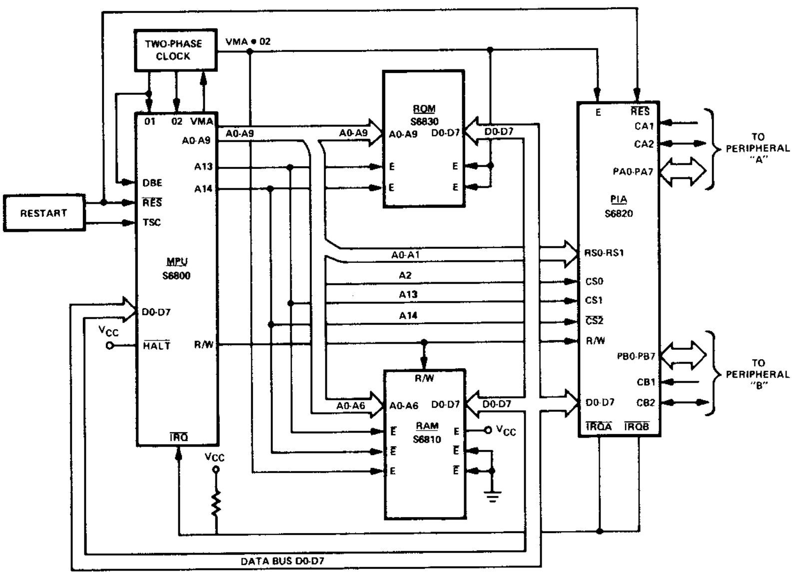
CHIP SELECTION AND ADDRESSING—The Minimum system configuration permits direct selection of the ROM, RAM, ACIA and PIA without the use of special TTL select logic. This is accomplished by simply wiring the address lines A13 A14 to the Enable or chip select lines on the memories and PIA. This permits the devices to be addressed as follows:

Device	A14	A13	Hex Addresses
RAM	0	0	0000–007F
PIA	0	1	2004–2007 (Registers)
ROM	1	1	6000–63FF

Other addressing schemes can be utilized which use any combination of two of the lines A10 through A14 for chip selection.

PERIPHERAL CONTROL—All control and timing for the peripherals that are connected to the PIA is accomplished by software routines under the control of the MPU.

FIGURE 3. MINIMUM SYSTEM IMPLEMENTATION

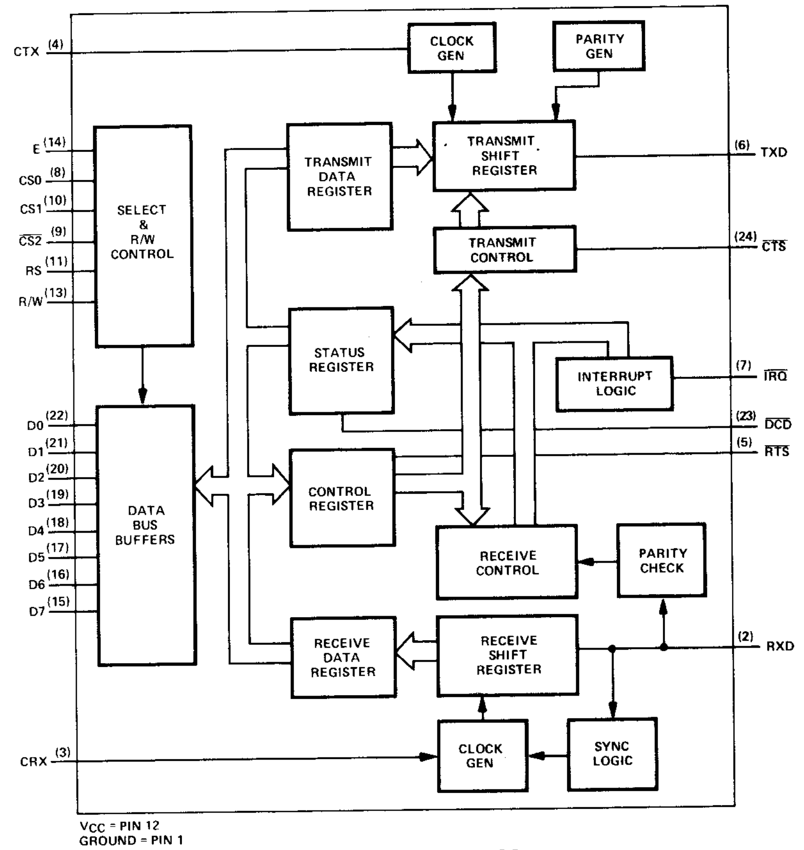


S6850

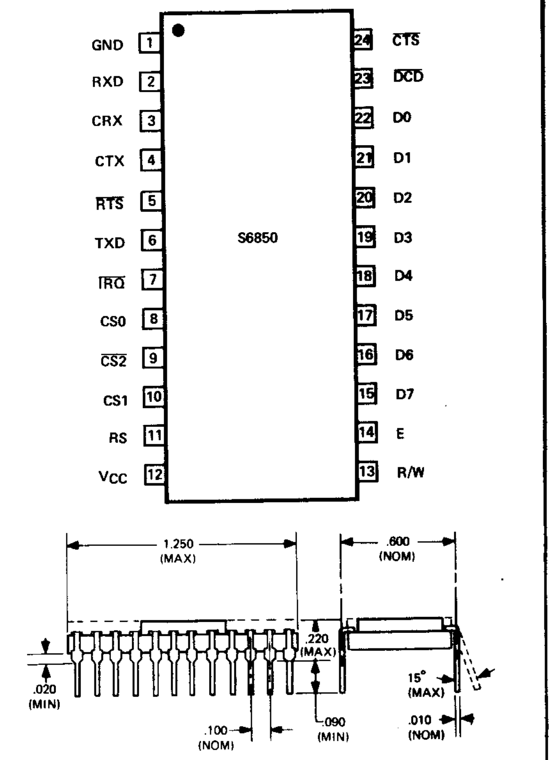
ASYNCHRONOUS COMMUNICATION
INTERFACE ADAPTER (ACIA)

AMERICAN MICROSYSTEMS, INC.

ADVANCED PRODUCT DESCRIPTION



BLOCK DIAGRAM



PIN/PACKAGE CONFIGURATION

FEATURES

- 8 Bit Bidirectional Data Bus for Communication with MPU.
- False start bit deletion.
- Peripheral/modem control functions.
- Double buffered Receiver and Transmitter
- One or two stop bit operation.
- Eight and nine-bit transmission with optional even and odd parity.
- Parity, overrun and framing error checking.
- Programmable control register.
- Optional ÷1, ÷16, and ÷64 clock modes.
- Up to 500,000 bps transmission.

FUNCTIONAL DESCRIPTION

The S6850 Asynchronous Communications Interface Adapter (ACIA) provides the data formatting and control to interface serial asynchronous data communications to bus organized systems such as the S6800 Microprocessing Unit.

The S6850 includes select enable, read/write, interrupt and bus interface logic to allow data transfer over an eight bit bi-directional data bus. The parallel data of the bus system is serially transmitted and received by the asynchronous data interface, with proper formatting and error checking. The functional configuration of the ACIA is programmed via the data bus during system initialization. Word lengths, clock division ratios and transmit control through the Request to Send output may be programmed. For modem operation three control lines are provided. These lines allow the ACIA to interface directly with the S6860 0-600 bps digital modem.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage V_{CC}	−0.3 to +7.0V	Operating Temperature Range T_A	0 to +70°C
Input Voltage V_{in}	−0.3 to +7.0V	Storage Temperature Range T_{stg}	−55 to +150°C

NOTE: This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields, however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

DC (STATIC) CHARACTERISTICS

(V_{CC} = 5.0V ± 5%, T_A = 25°C unless otherwise noted.)

Characteristic	Symbol	Min.	Typ.	Max.	Unit
Input High Voltage (Normal Operating Levels)	V_{IH}	+2.4	–	V_{CC}	Vdc
Input Low Voltage (Normal Operating Levels)	V_{IL}	−0.3	–	+0.4	Vdc
Input High Threshold Voltage — All Inputs Except Enable	V_{IHT}	+2.0	–	–	Vdc
Input Low Threshold Voltage — All Inputs Except Enable	V_{ILT}	–	–	+0.8	Vdc
Input Leakage Current (V_{in} = 0 to 5.0 Vdc) R/W, RS, CS0, CS1, $\overline{CS2}$, Enable	I_{in}	–	1.0	2.5	μAdc
Three-State (Off State) Input Current (V_{in} = 0.4 to 2.4 Vdc, V_{CC} = max) D0-D7,	I_{TSI}	–	2.0	10	μAdc
Output High Voltage (I_{Load} = −100 μAdc, Enable Pulse Width < 25 μs) All Outputs Except $\overline{IRQ}$	V_{OH}	+2.4	–	–	Vdc
Output Low Voltage (I_{Load} = 1.6 mAdc) Enable Pulse Width < 25 μs	V_{OL}	–	–	+0.4	Vdc
Output Leakage Current (Off State) $\overline{IRQ}$	I_{LOH}	–	1.0	10	μAdc
Power Dissipation	P_D	–	300	525	mW
Input Capacitance (V_{in} = 0, T_A = 25°C, f = 1.0 MHz)	C_{in}				pF
D0-D7		–	–	10	
R/W, RS, CS0, CS1, $\overline{CS2}$, RXD, CTX, CRX, $\overline{CTS}$, $\overline{DCD}$		–	–		
Enable		–	–	10	
Output Capacitance (V_{in} = 0, T_A = 25°C, f = 1.0 MHz)	C_{out}	–	–	10	pF

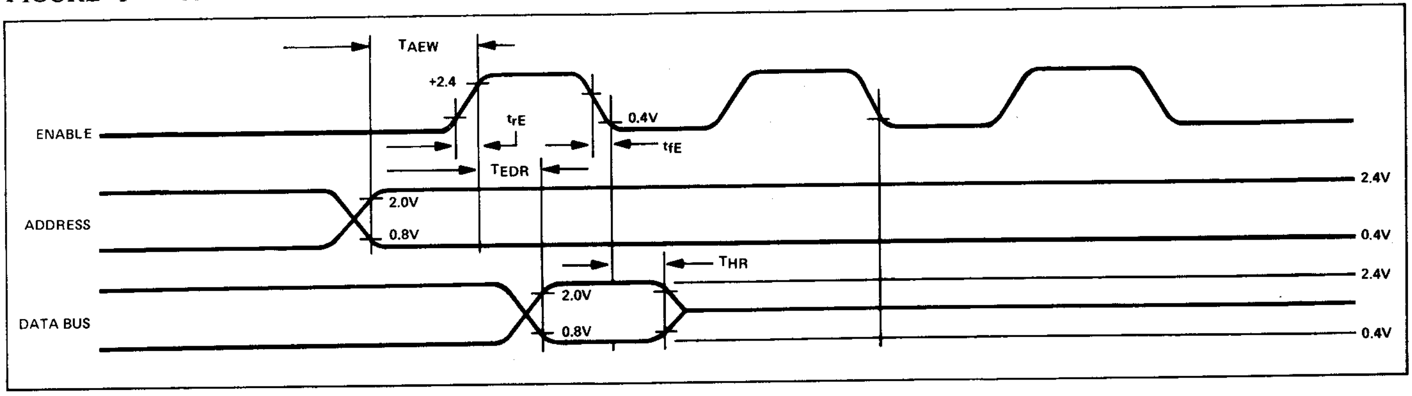
AC (DYNAMIC) CHARACTERISTICS

Loading = 130 pF and one TTL load for D0-D7 = 20pF and 1 TTL load for $\overline{RTS}$ and TXD = 100pF and 3KΩ to V_{CC} for $\overline{IRQ}$.

READ TIMING CHARACTERISTICS (Figure 1)

Characteristic	Symbol	Min.	Typ.	Max.	Unit
Setup Time, Address valid to Enable positive transition	T_{AEW}	180	–	–	ns
Setup Time, Enable positive transition to Data valid on bus	T_{EDR}	–	–	395	ns
Data Bus Hold Time	T_{HR}	10	–	–	ns
Rise and Fall Time for Enable input	t_{rE}, t_{fE}	–	–	25	μs

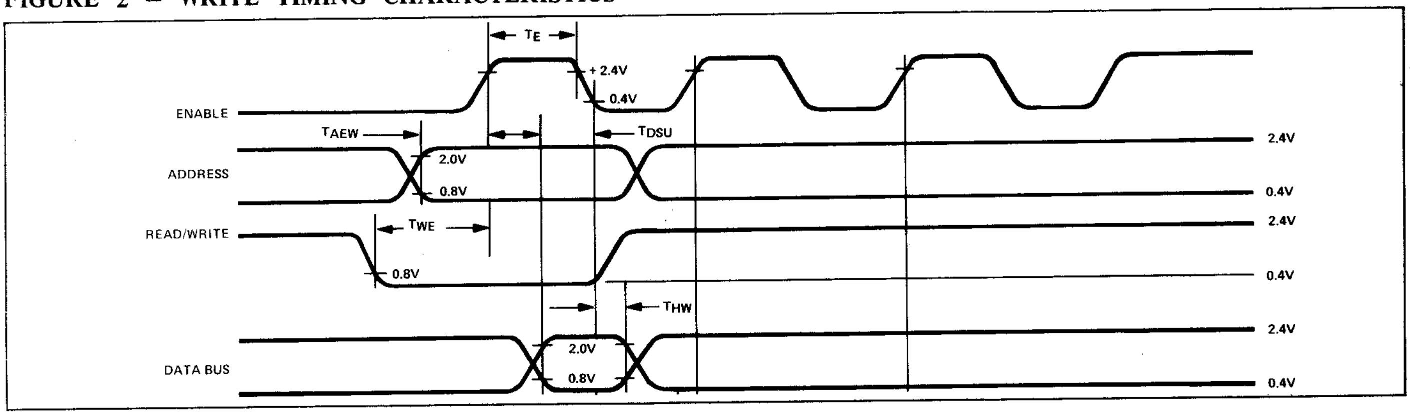
FIGURE 1 – READ TIMING CHARACTERISTICS



WRITE TIMING CHARACTERISTICS (Figure 2)

Characteristic	Symbol	Min.	Typ.	Max.	Unit
Enable Pulse Width	T_E	0.470	–	25	μs
Setup Time, Address valid to Enable positive transition	T_{AEW}	180	–	–	ns
Setup Time, Data valid to Enable netative transition	T_{DSU}	300	–	–	ns
Setup time, Read/Write negative transition to Enable positive transition	T_{WE}	130	–	–	ns
Data Bus Hold Time	T_{HW}	10	–	–	ns

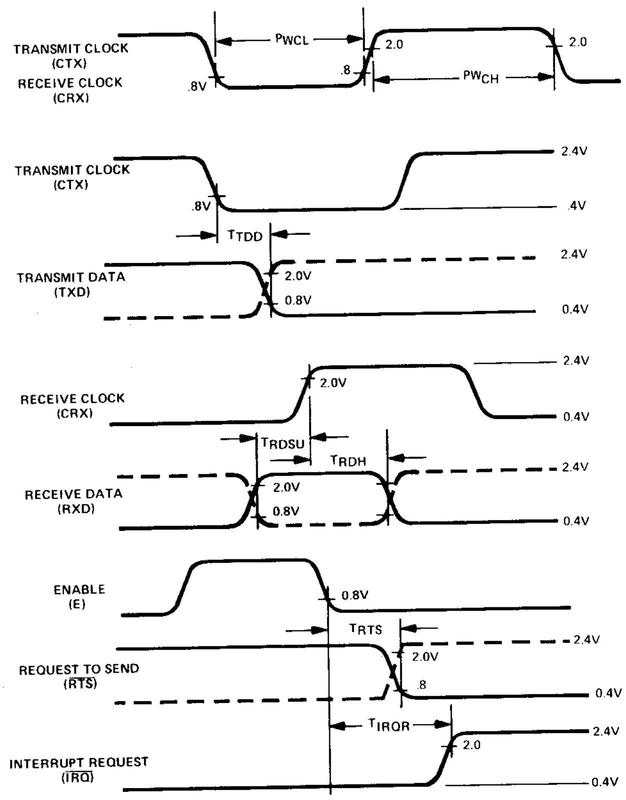
FIGURE 2 – WRITE TIMING CHARACTERISTICS



TRANSMIT/RECEIVE CHARACTERISTICS (Figure 3)

Characteristic	Symbol	Min.	Typ.	Max.	Unit
Clock Frequency ÷ 1 mode ÷ 16 mode ÷ 64 mode	f_C			500 800 800	KHz KHz KHz
Clock Pulse Width, Low State	PW_{CL}	600			nsec
Clock Pulse Width, High State	PW_{CH}	600			nsec
Delay Time, Transmit Clock to Data Out	T_{TDD}			1.0	μsec
Set up Time, Receive Data	T_{RDSU}	500			nsec
Hold Time, Receive Data	T_{RDH}	500			nsec
Delay Time, Enable to $\overline{IRQ}$ Reset	T_{IRQR}			1.2	μsec
Delay Time, Enable to $\overline{RTS}$	T_{RTS}			1.0	μsec

FIGURE 3 – TRANSMIT/RECEIVE TIMING



MPU/ACIA INTERFACE

Pin	Label	FUNCTION
(22) (21) (20) (19) (18) (17) (16) (15)	D0 D1 D2 D3 D4 D5 D6 D7	**ACIA BI-DIRECTIONAL DATA LINES**–The bi-directional data lines (D0-D7) allow for data transfer between the ACIA and the MPU. The data bus output drivers are three-state devices that remain in the high-impedance (off) state except when the MPU performs an ACIA read operation. The Read/Write line is in the read (high) state when the ACIA is selected for a read operation.
(14)	E	**ACIA ENABLE SIGNAL**–The Enable signal (E) is a high impedance TTL compatible input that enables the bus input/output data buffers and clocks data to and from the ACIA. This signal will normally be a derivative of the S6800 $\phi 2$ clock.
(13)	R/W	**READ/WRITE CONTROL SIGNAL**–The Read/Write line is a high impedance input that is TTL compatible and is used to control the direction of data flow through the ACIA's input/output data bus interface. When Read/Write is high (MPU Read cycle), the ACIA output driver is turned on and a selected register is read. When it is low, the ACIA output driver is turned off and the MPU writes into a selected register. Thus, the Read/Write signal is used to select the Read Only or Write Only registers within the ACIA.
(8) (10) (9)	CS0 CS1 $\overline{CS2}$	**CHIP SELECT SIGNALS**–These three high impedance TTL compatible input lines are used to address an ACIA. A particular ACIA is selected when CS0 and CS1 are high and $\overline{CS2}$ is low. Transfers of data to and from ACIA are then performed under the control of Enable, Read/Write, and Register Select.
(11)	RS	**REGISTER SELECT SIGNAL**–The Register Select line is a high impedance input that is TTL compatible and is used to select the Transmit/Receive Data or Control/Status registers in the ACIA. The Read/Write signal line is used in conjunction with Register Select to select the Read Only or Write Only register in each register pair.
(7)	$\overline{IRQ}$	**INTERRUPT REQUEST SIGNAL**–Interrupt request is a TTL compatible, open drain active low output that is used to interrupt the MPU. The Interrupt Request remains low as long as the cause of the interrupt is present and the appropriate interrupt enable within the ACIA is set.

ACIA/MODEM OR PERIPHERAL INTERFACE

Pin	Label	FUNCTION
(4)	CTX	**TRANSMIT CLOCK**–The Transmit Clock is a high impedance TTL compatible input used for the clocking of transmitted data. The transmitter initiates data on the negative transition of the clock. Clock frequency of 1, 16, or 64 times the data rate may be selected.

Pin	Label	FUNCTION
(3)	CRX	**RECEIVE CLOCK**–The Receive Clock is a high impedance TTL compatible input used for synchronization of received data. (In the ÷ 1 mode, the clock and data must be synchronized externally.) The receiver strobes the data on the positive transition of the clock. Clock frequency of 1, 16, or 64 times the data rate may be selected.
(2)	RXD	**RECEIVED DATA**–The Received Data line is a high impedance TTL compatible input through which data is received in a serial NRZ(Non Return to Zero) format. Synchronization with a clock for detection of data is accomplished internally when clock rates of 16 or 64 times the bit rate are used. Data rates are in the range of 0 to 500 Kbps when external synchronization is utilized.
(6)	TXD	**TRANSMIT DATA**–The Transmit Data output line transfers serial NRZ data to a modem or other peripheral device. Data rates are in the range of 0 to 500Kbps when external synchronization is utilized.
(24)	$\overline{CTS}$	**CLEAR-TO-SEND**–This high impedance TTL compatible input provides automatic control of the transmitting end of a communications link via the modem's "clear-to-send" active low output by inhibiting the Transmitter Data Register Empty status bit (TDRE).
(5)	$\overline{RTS}$	**REQUEST-TO-SEND**–The Request-to-Send output enables the MPU to control a peripheral or modem via the data bus. The active state is low. The Request-to-Send output is controlled by the contents of the ACIA control register.
(23)	$\overline{DCD}$	**DATA CARRIER DETECTED**–This high impedance TTL compatible input provides automatic control of the receiving end of a communications link by means of the modem "Data-Carrier-Detect" or "Received-Line-Signal Detect" output. The $\overline{DCD}$ input inhibits and initializes the receiver section of the ACIA when high. A low to high transition of the Data Carrier Detect initiates an interrupt to the MPU to indicate the occurrence of a loss of carrier when the Receiver Interrupt Enable (RIE) is set.
(12)	V_{CC}	**+5 volts ± 5%**
(1)	GND	**GROUND**

APPLICATION INFORMATION

INTERNAL REGISTERS–The ACIA has four internal registers utilized for status, control, receiving data, and transmitting data. The register addressing by the R/W and RS lines and the bit definitions for each register are shown in Figure 4.

FIGURE 4 – DEFINITION OF ACIA REGISTERS

	BUFFER ADDRESS			
	RS • $\overline{R/W}$	**RS • R/W**	**$\overline{RS}$ • $\overline{R/W}$**	**$\overline{RS}$ • R/W**
Data Bus Line Number	Transmit Data Register	Receiver Date Register	Control Register	Status Register
	(Write Only)	(Read Only)	(Write Only)	(Read Only)
0	Data Bit 0*	Data Bit 0*	Clk. Divide Sel. 1 (CR0)	Rx Data Reg. Full (RDRF)
1	Data Bit 1	Data Bit 1	Clk. Divide Sel. 2 (CR1)	Tx Data Reg. Empty (TDRE)
2	Data Bit 2	Data Bit 2	Word Sel. 1 (CR2)	$\overline{\text{Data Carrier Det.}}$ ($\overline{\text{DCD}}$)
3	Data Bit 3	Data Bit 3	Word Sel. 2 (CR3)	$\overline{\text{Clear-to-Send}}$ ($\overline{\text{CTS}}$)
4	Data Bit 4	Data Bit 4	Word Sel. 3 (CR4)	Framing Error (FE)
5	Data Bit 5	Data Bit 5	Tx Control 1 (CR5)	Receiver Overrun (OVRN)
6	Data Bit 6	Data Bit 6	Tx Control 2 (CR6)	Parity Error (PE)
7	Data Bit 7***	Data Bit 7**	Rx Interrupt Enable (CR7)	Interrupt Request (IRQ)

Notes:
* Leading bit = LSB = Bit 0
** Unused data bits in received character will be "0's."
*** Unused data bits for transmission are "don't care's."

ACIA STATUS REGISTER–Information on the status of the ACIA is available to the MPU by reading the ACIA Status Register. This Read Only register is selected when RS is low and R/W is high. Information stored in this register indicates the status of: transmitting data register, the receiving data register and error status and the modem status inputs of the ACIA.

Receiver Data Register Full (RDRF) [Bit 0] – Receiver Data Register Full indicates that received data has been transferred to the Receiver Data Register. RDRF is cleared after an MPU read of the Receiver Data Register or by a Master Reset. The cleared or empty state indicates that the contents of the Receiver Data Register are not current. Data Carrier Detect being high also causes RDRF to indicate empty.

Transmit Data Register Empty (TDRE) [Bit 1]–The Transmit Data Register Empty bit being set high indicates that the Transmit Data Register contents have been transferred and that new data may be entered. The low state indicates that the register is full and that transmission of a new character has not begun since the last write data command.

Data Carrier Detect ($\overline{DCD}$) [Bit 2] – The Data Carrier Detect bit will be high when the $\overline{DCD}$ input from a modem has gone high to indicate that a carrier is not present. This bit going high causes an Interrupt Request to be generated if the Receiver Interrupt Enable (RIE) is set. It remains high until the interrupt is cleared by reading the Status Register and the data register or a Master Reset occurs. If the $\overline{DCD}$ input remains high after Read Status and Read Data or Master Reset have occurred, the $\overline{DCD}$ Status bit remains high and will follow the $\overline{DCD}$ input.

Clear-to-Send ($\overline{CTS}$) [Bit 3] – The Clear-to-Send bit indicates the state of the Clear-to-Send input from a modem. A low $\overline{CTS}$ indicates that there is a Clear-to-Send from the modem. In the high state, the Transmit Data Register Empty bit is inhibited and the Clear-to-Send status bit will be high. Master Reset does not affect the Clear-to-Send status bit.

Framing Error (FE) [Bit 4] – Framing error indicates that the received character is improperly framed by the start and stop bit and is detected by the absence of the 1st stop bit. This error indicates a synchronization error, faulty transmission, or a break condition. The framing error flag is set or reset during the receiver data transfer time. Therefore, this error indicator is present throughout the time that the associated character is available.

Receiver Overrun (OVRN) [Bit 5] – Overrun is an error flag that indicates that one or more characters in the data stream were lost. That is, a character or a number of characters were received but not read from the Receiver Data Register (RDR) prior to subsequent characters being received. The overrun condition begins at the midpoint of the last bit of the second character received in succession without a read of the RDR having occurred. The Overrun does not occur in the Status Register until the valid character prior to Overrun has been read. The RDRF bit remains set until Overrun is reset. Character synchronization is maintained during the Overrun condition. The overrun indication is reset after the reading of data from the Receive Data Register. Overrun is also reset by the Master Reset.

Parity Error (PE) [Bit 6] –The parity error flag indicates that the number of highs (ones) in the character does not agree with the preselected odd or even parity. Odd parity is defined to be when the total number of ones is odd. The parity error indication will be present as long as the data character is in the RDR. If no parity is selected, then both the transmitter parity generator output and the receiver parity check results are inhibited.

Interrupt Request ($\overline{IRQ}$) [Bit 7] –The IRQ bit indicates the state of the $\overline{IRQ}$ output. Any interrupt that is set and enabled will be indicated in the status register. Any time the $\overline{IRQ}$ output is low the IRQ bit will be high to indicate the interrupt or service request status.

CONTROL REGISTER–The ACIA control Register consists of eight bits of write only buffer that are selected when RS and R/W are low. This register controls the function of the receiver, transmitter, interrupt enables, and the Request-to-Send modem control output.

Counter Divide Select Bits (CR0 and CR1)–The Counter Divide Select Bits (CR0 and CR1) determine the divide ratios utilized in both the transmitter and receiver sections of the ACIA. Additionally, these bits are used to provide a Master Reset for the ACIA which clears the Status Register and initializes both the receiver and transmitter. Note that after a power-on or a power-fail restart, these bits must be set High to reset the ACIA. After resetting, the clock divide ratio may be selected. These counter select bits provide for the following clock divide ratios:

CR1	CR0	Function
0	0	÷ 1
0	1	÷16
1	0	÷64
1	1	Master Reset

Word Select Bits (CR2, CR3, and CR4)–The Word Select bits are used to select word length, parity, and the number of stop bits. The encoding format is as follows:

CR4	CR3	CR2	Function
0	0	0	7 Bits + Even Parity + 2 Stop Bits
0	0	1	7 Bits + Odd Parity + 2 Stop Bit
0	1	0	7 Bits + Even Parity + 1 Stop Bit
0	1	1	7 Bits + Odd Parity + 1 Stop Bit
1	0	0	8 Bits + 2 Stop Bits
1	0	1	8 Bits + 1 Stop Bit
1	1	0	8 Bits + Even Parity + 1 Stop Bit
1	1	1	8 Bits + Odd Parity + 1 Stop Bit

Word length, Parity Select, and Stop Bit changes are not double-buffered and therefore become effective immediately.

Transmitter Control Bits (CR5 and CR6)–Two Transmitter Control bits provide for the control of the Transmitter Buffer Empty interrupt output, the Request-to-Send output and the transmission of a BREAK level (space). The following encoding format is used:

CR6	CR5	Function
0	0	$\overline{RTS}$ = low, Transmitting Interrupt Disabled
0	1	$\overline{RTS}$ = low, Transmitting Interrupt Enabled
1	0	$\overline{RTS}$ = high, Transmitting Interrupt Disabled
1	1	$\overline{RTS}$ = low, Transmitting Interrupt Disabled and Transmits a BREAK level on the Transmit Data Output.

Receiver Interrupt Enable Bit (RIE) (CR7)–Interrupts will be enabled by a high level in bit position 7 of the Control Register (CR7). Interrupts caused by the Receiver Data Register Full being high or by a low to high transition on the Data Carrier Detect signal line are enabled or disabled by the Receiver Interrupt Enable Bit.

TRANSMIT DATA REGISTER (TDR)–Data is written in the Transmit Data Register *during* the peripheral enable time (E) when the ACIA has been addressed and RS • R/W is selected. Writing data into the register causes the Transmit Data Register Empty bit in the status register to go low. Data can then be transmitted. If the transmitter is idling and no character is being transmitted, then the transfer will take place within one bit time of the trailing edge of the Write command. If a character is being transmitted, the new data character will commence as soon as the previous character is complete. The transfer of data causes the Transmit Data Register Empty (TDRE) bit to indicate empty.

RECEIVE DATA REGISTER (RDR)–Data is automatically transferred to the empty Receive Data Register (RDR) from the receiver deserializer (a shift register) upon receiving a complete character. This event causes the Receiver Data Register Full bit (RDRF) (in the status buffer) to go high (full). Data may then be read through the bus by addressing the ACIA and selecting the Receiver Data Register with RS and R/W high when the ACIA is enabled. The non-destructive read cycle causes the RDRF bit to be cleared to empty although the data is retained in the RDR. The status is maintained by RDRF as to whether or not the data is current. When the Receiver Data Register is full, the automatic transfer of data from the Receiver Shift Register to the Data Register is inhibited and the RDR contents remain valid with its current status stored in the Status Register.

OPERATIONAL DESCRIPTION

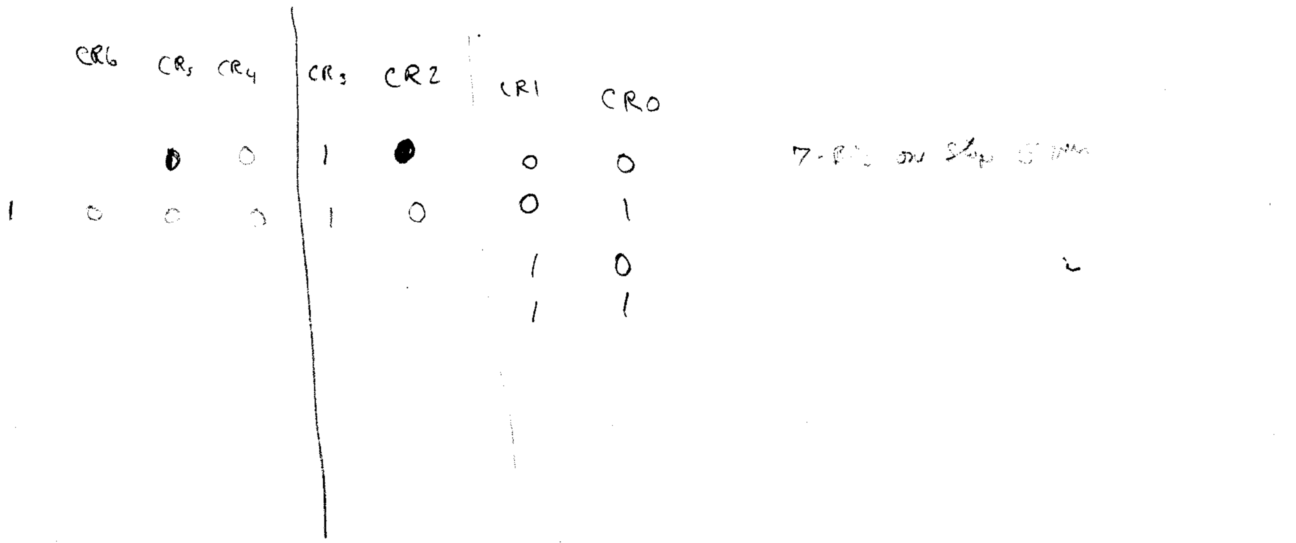
From the MPU Bus interface the ACIA appears as two addressable RAM memory locations. Internally, there are four registers; two read-only and two write-only registers. The read-only registers are status and receive data, and the write only registers are control and transmit data. The serial interface consists of serial transmit and receive lines and three modem/peripheral control lines.

During a power-on sequence, the ACIA is internally latched in a reset condition to prevent erroneous output transitions. This power-on reset latch can only be released by the master reset function via the control register; bits b_0 and b_1 are set "high" for a master reset. After master resetting the ACIA, the programmable control register can be set for a number of options such as variable clock divider ratios, variable word length, one or two stop bits, parity (even, odd, or none) and etc.

TRANSMITTER–A typical transmitting sequence consists of reading the ACIA status register either as a result of an interrupt or in the ACIA's turn in a polling sequence. A character may be written into the Transmitter Data Register if the status read operation has indicated that the Transmit Data

Register is empty. This character is transferred to a shift register where it is serialized and transmitted from the Tx Data output preceded by a start bit and followed by one or two stop bits. Internal parity (odd or even) can be optionally added to the character and will occur between the last data bit and the first stop bit. After the first character is written in the data register, the status register can be read again to check for a Transmit Data Register Empty condition and current peripheral status. If the register is empty, another character can be loaded for transmission even though the first character is in the process of being transmitted. This second character will be automatically transferred into the shift register when the first character transmission is completed. The above sequence continues until all the characters have been transmitted.

RECEIVER–Data is received from a peripheral by means of the Rx Data input. A divide by one clock ratio is provided for an externally synchronized clock (to its data) while the divide by 16 and 64 ratios are provided for internal synchronization. Bit synchronization in the divide by 16 and 64 modes is obtained by the detection of the leading mark-to-space transition of the start bit. False start bit deletion capability insures that a full half bit of a start bit has been received before the internal clock is synchronized to the bit time. As a character is being received, parity (odd or even) will be checked and the error indication will be available in the status register along with framing error, overrun error, and receiver data register full. In a typical receiving sequence, the status register is read to determine if a character has been received from a peripheral. If the receiver data register is full, the character is placed on the 8-bit ACIA bus when a Read Data command is received from the MPU. The status register can be read again to determine if another character is available in the receiver data register. The receiver is also double buffered so that a character can be read from the data register as another character is being received in the shift register. The above sequence continues until all characters have been received.

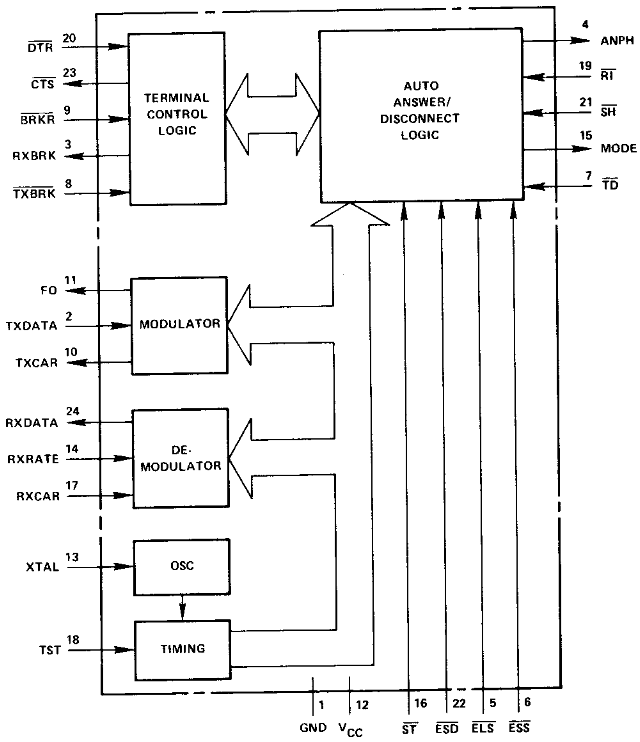


S6860

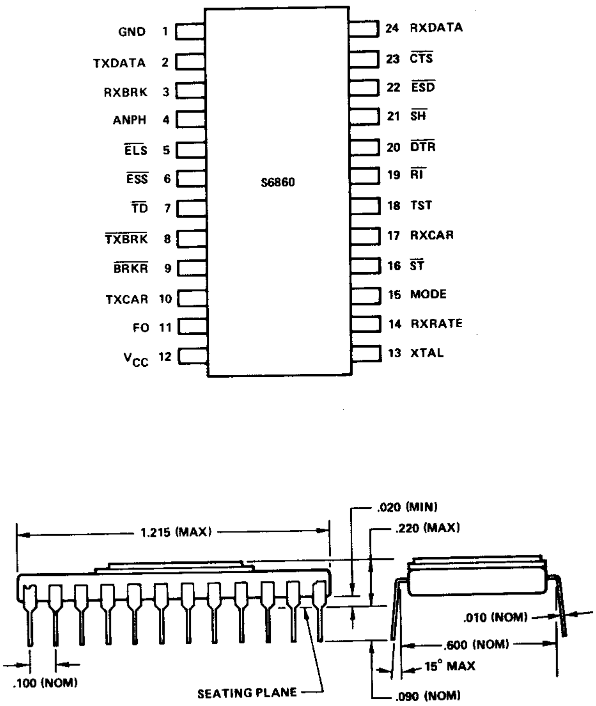
0-600 BPS
DIGITAL MODEM

AMERICAN MICROSYSTEMS, INC.

ADVANCED PRODUCT DESCRIPTION



BLOCK DIAGRAM



PIN/PACKAGE CONFIGURATION

FEATURES

- Full or half duplex operation
- Originate and answer mode
- Auto answer and disconnect
- Modem self test
- TTL compatible terminal interfaces
- Crystal/External reference control
- Compatible functions for 100 series data sets and 1001 A/B data couplers

FUNCTIONAL DESCRIPTION

The S6860 is a 0-600 bps Digital Modem circuit designed to be integrated into a wide range of equipment utilizing serial data communications.

The modem provides the necessary modulation, demodulation and supervisory control functions to implement a serial data communications link, over a voice grade channel, utilizing frequency shift keying (FSK) a bit rates up to 600 bps. The S6860 can be implemented into a wide range of data handling systems, including stand alone modems, data storage devices, remote data communication terminals and I/O interfaces for minicomputers.

N-channel silicon gate technology permits the S6860 to operate using a single voltage supply and be fully TTL compatible.

The modem is compatible with the S6800 microcomputer family, interfacing directly with the Asynchronous Communications Interface Adapter (ACIA) to provide low-speed data communications capability.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage V_{CC}	- 0.3 to +7.0V	Operating Temperature Range T_A	0 to 70°C
Input Voltage V_{IN}	- 0.3 to +7.0V	Storage Temperature Range T_{STG}	- 50 to 150°C

NOTE: This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields, however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

DC (STATIC) CHARACTERISTICS

(V_{CC} = 5.0V ± 5%, T_A = 25°C unless otherwise noted.)

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNIT
V_{IH}	Input High Voltage, All inputs Except Crystal	2.0	–	V_{CC}	Vdc
V_{IL}	Input Low Voltage, All inputs Except Crystal	-0.3	–	0.8	Vdc
V_{IN}	Crystal Input Voltage (Crystal Input Driven from an External Reference, Input Coupling Capacitor = 200 pF, Duty Cycle = 50 ± 5%)	1.5	–	2.0	V_{p-p}
I_{IN}	Input Current				mAdc
	(V_{IN} = GND) All Inputs Except RXCAR,TXDATA, $\overline{TD}$, TST, $\overline{RI}$, $\overline{SH}$	–	–	-0.2	
	$\overline{RI}$, $\overline{SH}$ Inputs	–	–	-1.6	
I_{IL}	Input Leakage Current (V_{IN} = 0 to 5.0 Vdc)	–	–	1.	μAdc
V_{OH1}	Output High Voltage, All Outputs Except ANPH and TXCAR (I_{OH1} = -0.04 mAdc, Load A)	2.4	–	V_{CC}	Vdc
V_{OL1}	Output Low Voltage, All Outputs Except ANPH and TXCAR (I_{OL1} = 1.6 mAdc, Load A)	-0.3	–	0.4	Vdc
I_{OH2}	Output High Current, ANPH (V_{OH2} = 0.8 Vdc, Load B)	0.3	–	–	mAdc
V_{OL2}	Output Low Voltage, ANPH (I_{OL2}) = 0, Load B)	-0.3	–	0.3	Vdc
C_{IN}	Input Capacitance (f = 0.1 MHz)	–	5.	–	pF
C_{OUT}	Output Capacitance (f = 0.1 MHz)	–	10	–	pF
V_{CO}	Transmit Carrier Output Voltage (Load C)	0.20	0.35	0.50	V(RMS)
V_{2H}	Transmit Carrier Output 2nd Harmonic (Load C)	-25	-32	–	dB
I_{DD}	V_{CC} Supply Current (All Inputs at GND & All Outputs Open)	–	30	65	mAdc

AC (DYNAMIC) CHARACTERISTICS

(Loading is as shown in Figure 1 unless otherwise noted.)

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNIT
t_r t_f	Input Transition Times, All Inputs Except Crystal (Operating in the Crystal Input Mode; from 10% to 90% Points)	– –	– –	1.* 1.*	μs
t_r t_f	Input Transition Times, Crystal Input (Operating in External Input Reference Mode)	– –	– –	30 30	ns
t_r t_f	Output Transition Times, All Outputs Except TXCAR (From 10% to 90% Points)	– –	– –	5. 5.	μs

*Maximum Input Transition Times are ≤0.1 x Pulse Width or the specified maximum of 1.0 μs, whichever is smaller.

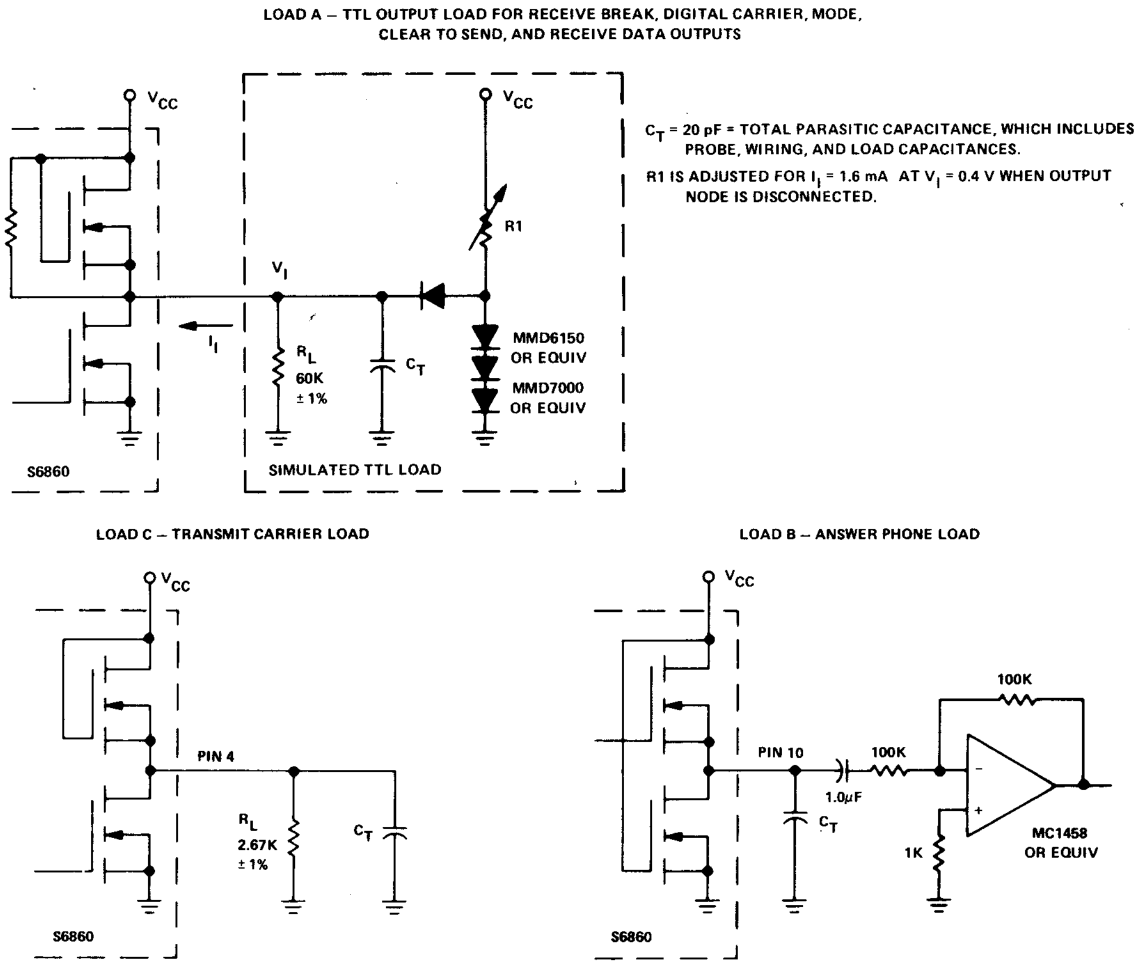


FIGURE 1 TEST LOADING

MODEM/TERMINAL INTERFACE

PIN	LABEL	FUNCTION
(2)	TXDATA	**Transmit Data** – Serial data transferred to the modem via the ACIA for transmitting to the receiving terminal.
(8)	$\overline{TXBRK}$	**Transmit Break** – Used to signal the remote modem to stop transmitting data. A $\overline{\text{Transmit Break (low)}}$ greater than 34 ms forces the modem to send a continuous space signal for 233 ms. $\overline{\text{Transmit Break}}$ must be initiated only after $\overline{CTS}$ has been established. This is a negative edge sense input. Prior to initiating $\overline{TXBRK}$ this input must be held high for a minimum of 34 ms.
(24)	RXDATA	**Receive Data** – The data resulting from demodulating the Receive Carrier signal. A high level is a mark.
(3)	RXBRK	**Receive Break** – Upon receipt of a continuous 150 ms space, the modem automatically clamps the Receive Break output high. This output is also clamped high until $\overline{\text{Clear-to-Send}}$ is established.
(9)	$\overline{BRKR}$	**Break Release** – The Receive Break output (clamp high condition) can be removed by holding the Break Release signal low for at least 20 μs after receiving a minimum 150 ms space signal.
(20)	$\overline{DTR}$	**Data Terminal Ready** – Enables the modem function when low. When $\overline{DTR}$ is held high for 34 ms minimum, a disconnect is initiated and will occur 3 sec. later.
(23)	$\overline{CTS}$	**Clear-to-Send** – A low on the $\overline{CTS}$ output indicates the Transmit Data input has been unclamped from a steady Mark, thus allowing data transmission.
(16)	$\overline{ST}$	**Self Test** – With this input at a low level, the demodulator is switched to the modulator frequency and demodulates the transmitted FSK signal. Channel establishment, which occurred during the initial handshake, is not lost during self test. The Mode Control output changes state during $\overline{\text{Self Test}}$, permitting the receive filters to pass the local Transmit Carrier.

$\overline{ST}$	$\overline{SH}$	$\overline{RI}$	MODE
H	L	H	H
H	H	L	L
L	L	H	L
L	H	L	H

PIN	LABEL	FUNCTION
(18)	TST	**Test Clock** – A high input signal decreases the modem test time. This input **must be low** for normal operation.
(11)	FO	**Frequency Output** – A test signal is output to decrease modem test time. The signal is a square wave at the transmit frequency.

EXTERNAL MODEM INTERFACE

PIN	LABEL	FUNCTION
(12)	V_{CC}	+ 5 Volts ± 5%
(1)	GND	**Ground**
(22)	$\overline{ESD}$	**Enable Space Disconnect** – When $\overline{ESD}$ is strapped low and $\overline{DTR}$ is pulsed to initiate a disconnect, the modem transmits a space for either 3 s or until a loss of threshold is detected, whichever occurs first. If $\overline{ESD}$ is strapped high, data instead of a space is transmitted. A disconnect occurs at the end of 3 s.
(5)	$\overline{ELS}$	**Enable Long Space Disconnect** – A strapping option which, when low, will automatically hang up the phone upon receipt of a continuous space for 1.5 s.
(6)	$\overline{ESS}$	**Enable Short Space Disconnect** – A strapping option which, when low, will automatically hang up the phone upon receipt of a continuous space for 0.3 s. **$\overline{ESS}$ and $\overline{ELS}$ must not be simultaneously strapped low.**
(13)	XTAL	**Crystal** – A 1.0 MHz crystal is required to use the on-chip oscillator. A 1.0 MHz square wave can also be applied to this pin to satisfy the clock requirements. Crystal parameteres are as follows:

Mode:	Parallel
Frequency:	1.0 MHz ± 0.1%
Series Resistance:	750 ohms max
Shunt Capacitance:	7.0 pF max
Temperature:	0 - 70°C
Test Level:	1.0 mW
Load Capacitance:	13 pF

When using the 1.0 MHz crystal, external parasitic capacitance, including crystal shunt capacitance, must be ⩽ 9 pF at the crystal input.

PIN	LABEL	FUNCTION
(14)	RXRATE	**Receive Data Rate** – The demodulator has been optimized for signal-to-noise performance at 300 bps and 600 bps. The Receive Data Rate input must be low for 0-600 bps and should be high for 0-300 bps.

MODEM/DATA COUPLER INTERFACE

PIN	LABEL	FUNCTION
(15)	MODE	**Mode** – Indicates the Originate (high) or Answer (low) status of the modem. This output changes when a Self Test ($\overline{ST}$) signal is applied.

MODEM/DATA COUPLER INTERFACE (Continued)

PIN	LABEL	FUNCTION
(19)	$\overline{RI}$	**Ring Indicator** – The modem function will recognize the receipt of a call from the CBT if at least 20 cycles of the 20 - 47 Hz ringing signal (low level ≥ 50% of the duty cycle) are present. The CBS $\overline{RI}$ signal must be level-converted to TTL according to the EIA RS-232 specification before interfacing it with the modem function. The receipt of a call from the CBS is recognized if the $\overline{RI}$ signal is present for at least 51 ms. This input is held high except during ringing. A $\overline{RI}$ signal automatically places the modem function in the Answer Mode.
(21)	$\overline{SH}$	**Switch Hook** – Interfaces directly with the CBT type Data Coupler and via the EIA RS-232 level conversion for the CBS type. An $\overline{SH}$ signal automatically places the modem function in the Originate Mode. $\overline{SH}$ is low during origination of a call. The modem will automatically hang up 17 s after releasing $\overline{SH}$ if the handshaking routine has not been accomplished.
(4)	ANPH	**Answer Phone** – Upon receipt of $\overline{\text{Ring Indicator}}$ or $\overline{\text{Switch Hook}}$ signal and $\overline{\text{Data Terminal Ready}}$, the Answer Phone output goes high ($[\overline{SH} + \overline{RI}] \bullet \overline{DTR}$). This signal drives the base of a transistor which activates the Off Hook and Data Transmission control lines in the data coupler. Upon call completion, the Answer Phone signal returns to a low level.
(7)	$\overline{TD}$	**Threshold Detect** – This input is derived from an external threshold detector. If the signal level is sufficient, the $\overline{TD}$ input must be low for 20 μs at least once every 32 ms to maintain normal operation. An insufficient signal level indicates the absence of the Receive Carrier; an absence for less than 32 ms will not cause channel establishment to be lost; however, data during this interval will be invalid. If the signal is present and the level is acceptable at all times, then the threshold input can be low permanently. Loss of threshold for 51 ms or longer results in a loss of Cler-to-Send. The Transmit Carrier of the originate modem is clamped off and a constant Mark is transmitted from the answer modem.
(17)	RXCAR	**Receive Carrier** – The FSK input to the demodulators. The local Transmit Carrier must be balanced or filtered out prior to this input, leaving only the Receive Carrier in the signal. The Receive Carrier must also be hard limited. Any half cycle period greater than or equal to 429 ± 1.0 μs for the low band or 235 ± 1.0 μs for the high band is detected as a space.

MODEM/DATA COUPLER INTERFACE (Continued)

PIN	LABEL	FUNCTION
(10)	TXCAR	**Transmit Carrier** – A digitally synthesized sine wave derived from a 1.0 MHz crystal reference (see Figure 2). Frequency characteristics are given in the following table.

MODE	DATA	FREQUENCY	TOLERANCE*
Originate	Mark	1270 Hz	- 0.15 Hz
Originate	Space	1070 Hz	- 0.09 Hz
Answer	Mark	2225 Hz	- 0.31 Hz
Answer	Space	2025 Hz	- 0.71 Hz

*The reference frequency tolerance is not included.

The proper output frequency is transmitted within 3.0 μs following a data bit change with no more than 2.0 μs phase discontinuity. The typical output level is 0.35 V (RMS) into a 100K-ohm load impedance.

The second harmonic is typically 32 dB below the fundamental (see Figure 3).

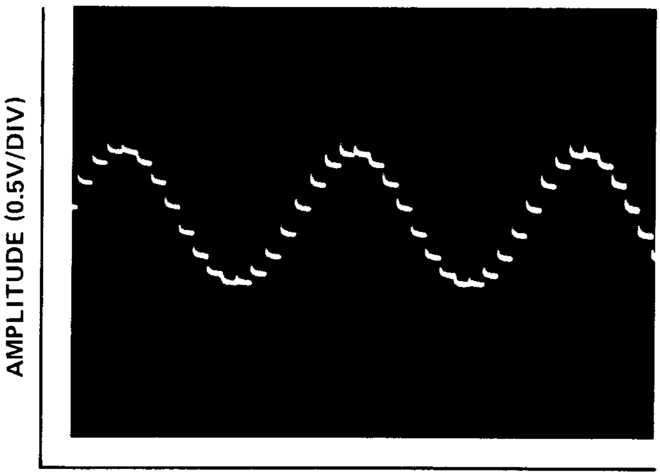


FIGURE 2 TRANSMIT CARRIER SINE WAVE

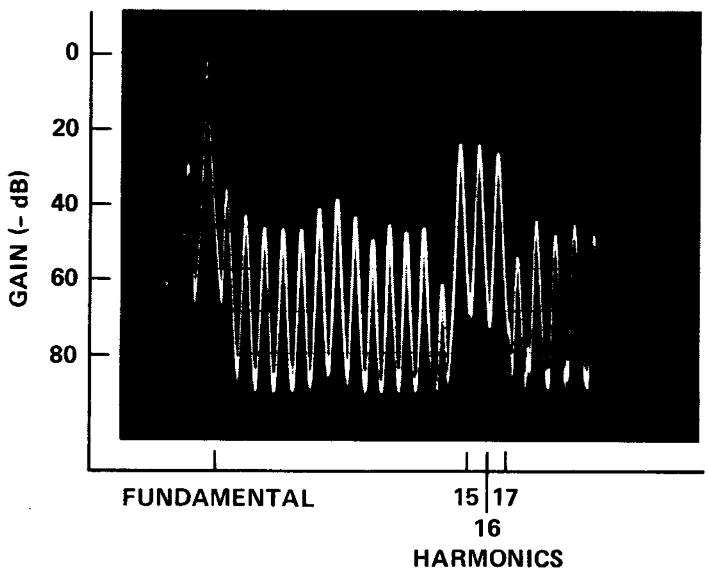


FIGURE 3 TRANSMIT CARRIER FREQUENCY SPECTRUM

OPERATIONAL DESCRIPTION

A typical configuration showing the S6860 modem and associated interconnections is shown in Figure 4. The transmit data is presented in serial format to the modulator for conversion to FSK signals for transmission on the telephone line. The modulator output is buffered before driving the line.

The incoming FSK signal from the remote modem is filtered to remove extraneous signals such as the local Transmit Carrier. This filtering can be either a bandpass which passes only the desired band of frequencies or a notch which rejects the known interferring signal. The desired signal is then limited to preserve the axis crossings and fed to the demodulator where the data is recovered from the received FSK carrier.

The Supervisory Control provides the necessary commands and responses for handshaking with the remote modem, along with the interface signals to the data coupler and communication terminal. If the modem is a built-in unit all input-output (I/O) logic need not be RS-232 compatible. However, if the modem is a stand-alone unit the computer-modem I/O interface must conform to the EIA specification. Line driver and receiver modules must be used to provide the required interface.

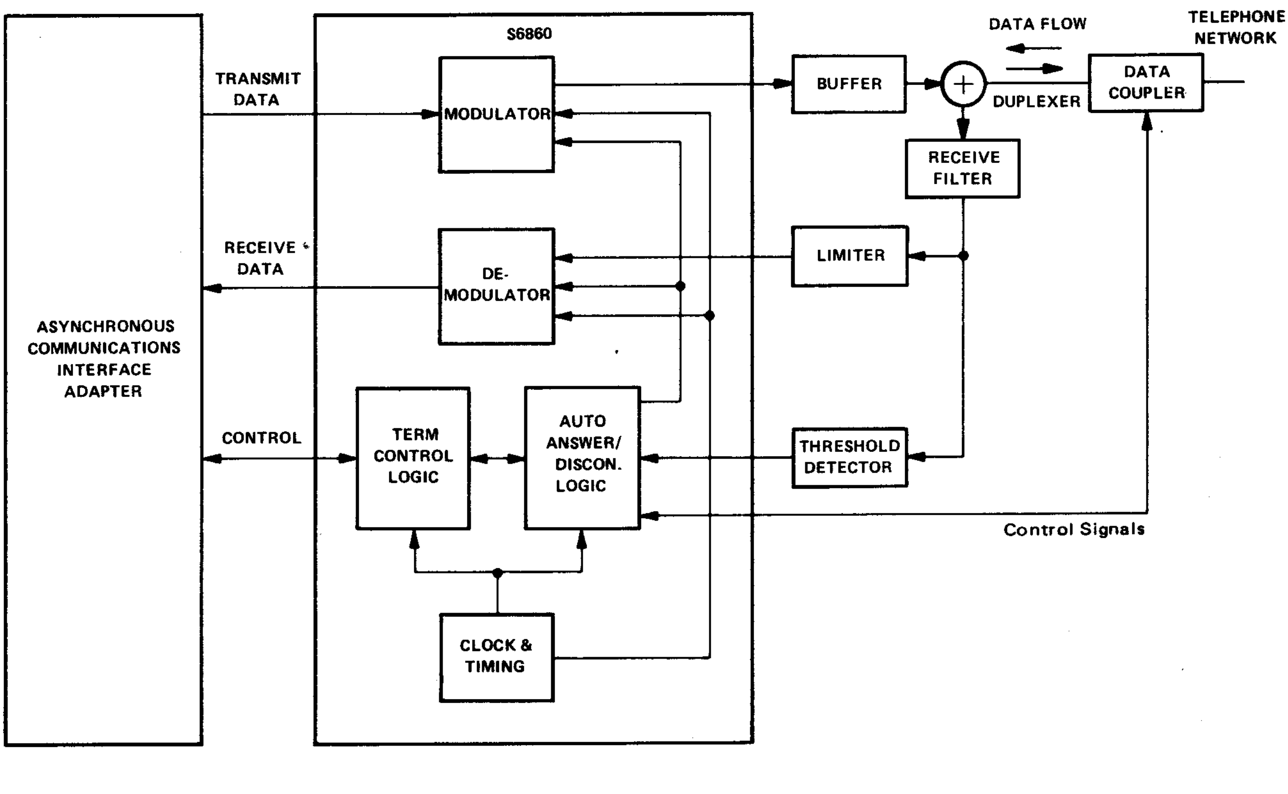


FIGURE 4 TYPICAL S6860 MODEM CONFIGURATION

Originate Mode

When a Switch Hook (SH) command is received, modem function is placed in the Originate Mode. If the Data Terminal Ready input is enabled (low) the modem will provide a logic high output at Answer Phone. The modem is now ready to receive the 2225 Hz Transmit Carrier signal from the remote answering modem. It will continue to look for this signal until 17 s after SH has been released. Disconnect occurs if the handshaking routine is not established.

Upon receiving 2225 ± 100 Hz for 150 ms at an acceptable amplitude, the Receive Data output is unclamped from a Mark condition and data reception can be accomplished. 450 ms after receiving a 2225 Hz signal, a 1270 Hz signal is transmitted to the remote modem. 750 ms after receiving the 2225 Hz signal, the Clear-to-Send output is taken low and data can now be transmitted as well as received.

Answer Mode

Automatic answering is first initiated by a receipt of a Ring Indicator (RI) signal from the Data Coupler. This can be either a low level for at least 51 ms as would come from a CBS data coupler, or at least 20 cycles of a 20 - 47 Hz ringing signal (low level ⩾ 50% of the duty cycle) as would come from a CBT data coupler. The presence of the Ring Indicator signal places the modem in the Answer Mode; If the Data Terminal Ready line is low, indicating the communication terminal is ready to send or receive data, the Answer Phone output goes high. This output is designed to drive a transistor switch which will activate the Off Hook (OH) and Data Transmission (DA) relays in the data coupler. Upon answering the phone the 2225 Hz Transmit Carrier is turned on.

The originate modem at the other end detects this 2225 Hz signal and after a 450 ms delay (used to disable any echo suppressors in the telephone network) transmits a 1270 Hz signal which the local answering modem detects, provided the amplitude and frequency requirements are met. The amplitude threshold is set external to the modem chip. If the signal level is sufficient the TD input should be low for 20 μs at least once every 32 ms. The absence of a threshold indication for a period greater than 51 ms denotes the loss of Receive Carrier and the modem begins hang-up procedures. Hang-up will occur 17 s after RI has been released provided the handshaking routine is not re-established. The frequency tolerance during handshaking is ± 100 Hz from the Mark frequency.

After the 1270 Hz signal has been received for 150 ms, the Receive Data is unclamped from a Mark condition and data can be received. The Clear-to-Send output goes low 450 ms after the receipt of carrier and data is transmitted to the answer modem.

Automatic Disconnect

A space frequency of 150 ms or greater duration on the line causes the modem to clamp the Receive Break high. This condition exists until a Break Release command is issued at the receiving station. Upon receipt of a 0.3 s space, with Enable Short Space Disconnect at the most negative voltage (low), the modem automatically hangs up. If Enable Long Space Disconnect is low, the modem requires 1.5 s of continuous space to hang up. Automatic Disconnect only occurs if the Enable Space Disconnect option is specified.

Initiate Disconnect

In order to command the remote modem to automatically hang up, a disconnect signal is sent by the local modem. This is accomplished by pulsing the normally low Data Terminal Ready into a high state for greater than 34 ms. The local modem then sends a 3 s continuous space and hangs up provided the Enable Space Disconnect is low. If the remote modem hangs up before 3 s, loss of Threshold Detect will cause loss of Clear-to-Send, which marks the line in Answer Mode and turns the carrier off in the Originate Mode.

If ESD is high the modem will transmit data until hang-up occurs 3 s later. Transmit Break is clamped 150 ms following the Data Terminal Ready interrupt.

INPUT/OUTPUT FUNCTIONS

Figure 5 shows the I/O interface for the S6860 modem.

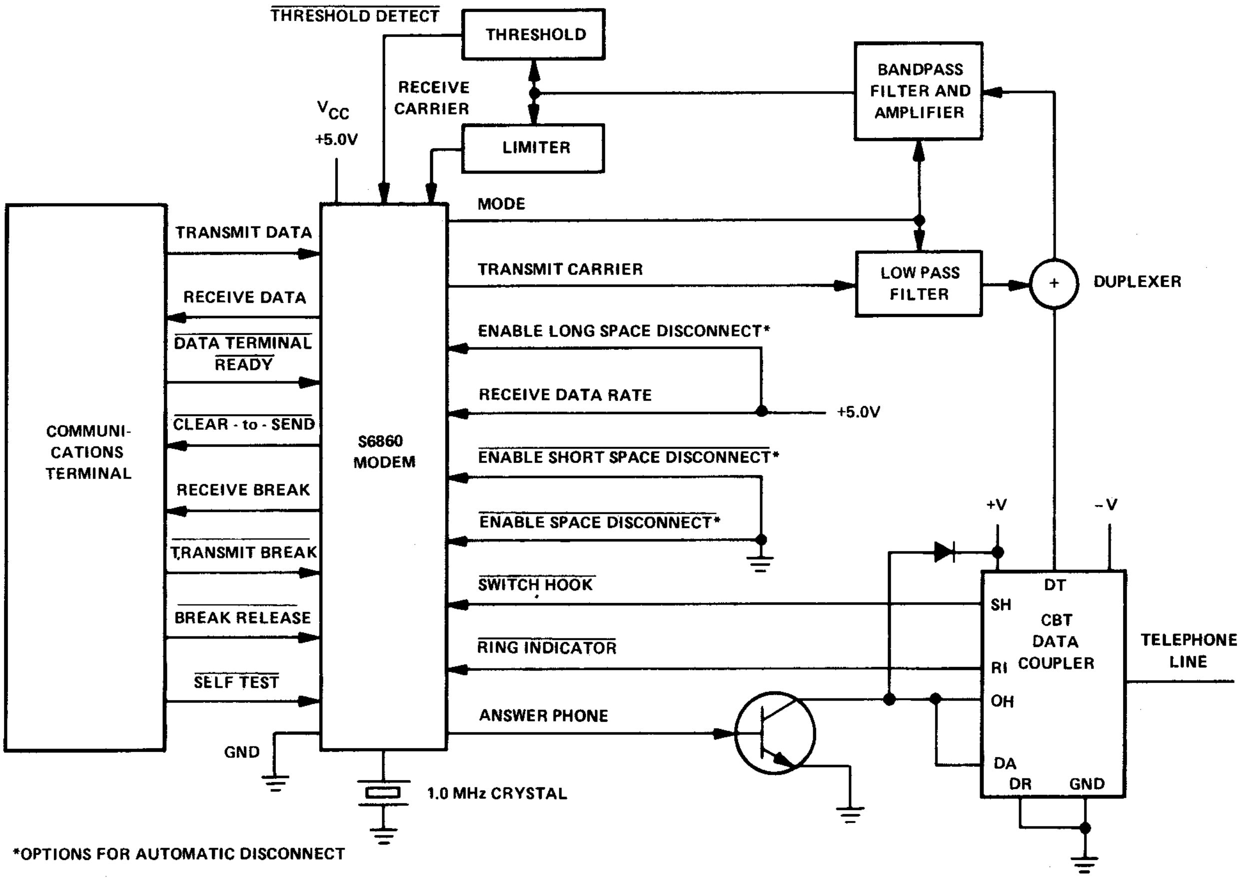


FIGURE 5 S6860 I/O INTERFACE CONNECTIONS

POWER-ON RESET

Power-on reset is provided on-chip to insure that when power is first applied the Answer Phone output is in the low (inactive) state. This holds the modem in the inactive or idle mode until a $\overline{SH}$ or $\overline{RI}$ signal has been applied. Once power has been applied, a momentary loss of power at a later time may not be of sufficient time to guarantee a chip reset through the power-on reset circuit.

To insure initial power-on reset action, the external parasitic capacitance on $\overline{RI}$ and $\overline{SH}$ should be $<$ 30 pF. Capacitance values $>$ 30 pF may require the use of an external pullup resistor to V_{CC} on these inputs in addition to the pull-up devices already provided on chip.

TIMING DIAGRAMS

Timing diagrams for Originate, Answer, Initiate Disconnect and Automatic Disconnect are shown in Figures 6, 7, 8 and 9 respectively. Timing delay variations are given in Tables I and II.

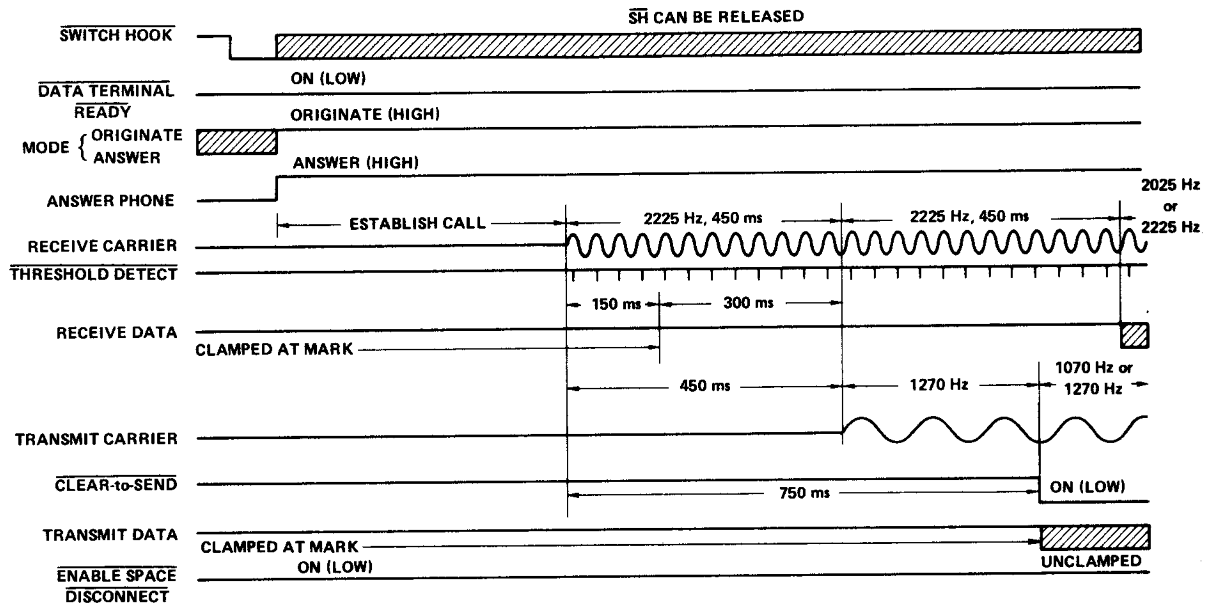


FIGURE 6 ORIGINATE MODE

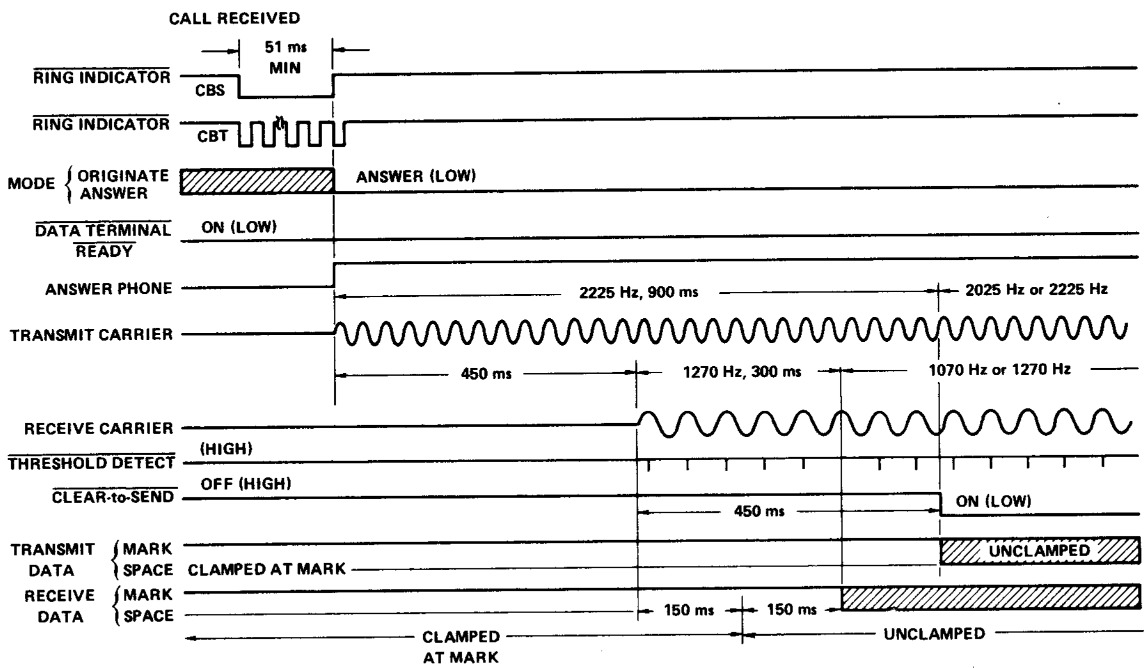


FIGURE 7 ANSWER MODE

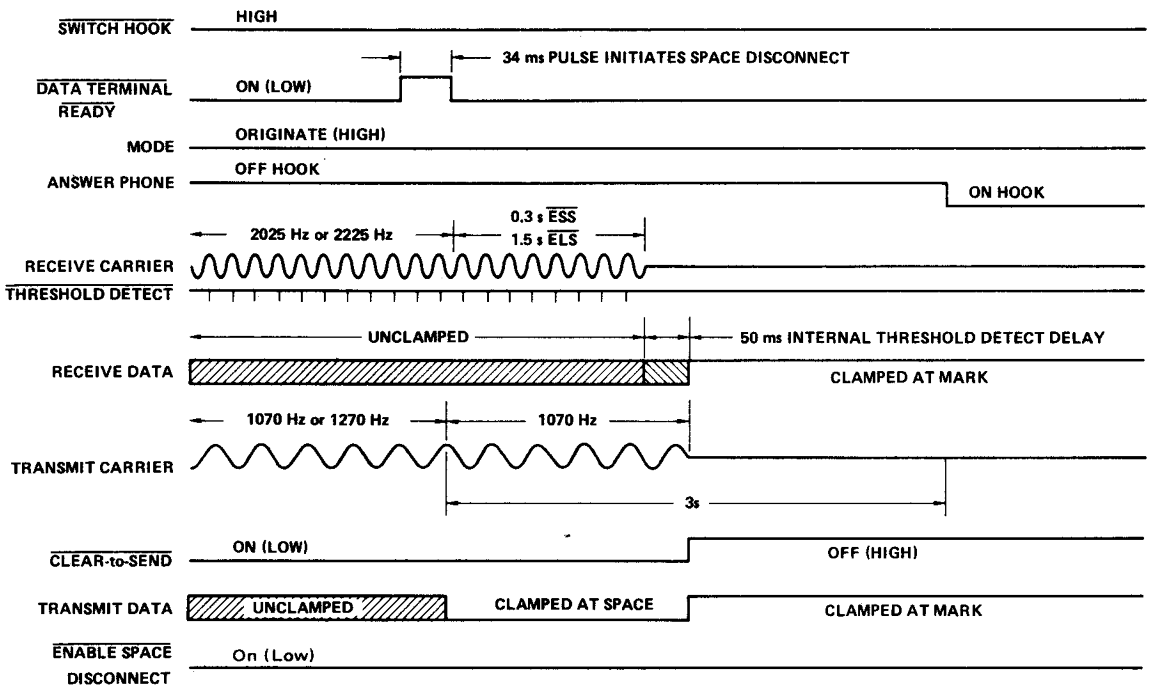


FIGURE 8 INITIATE DISCONNECT

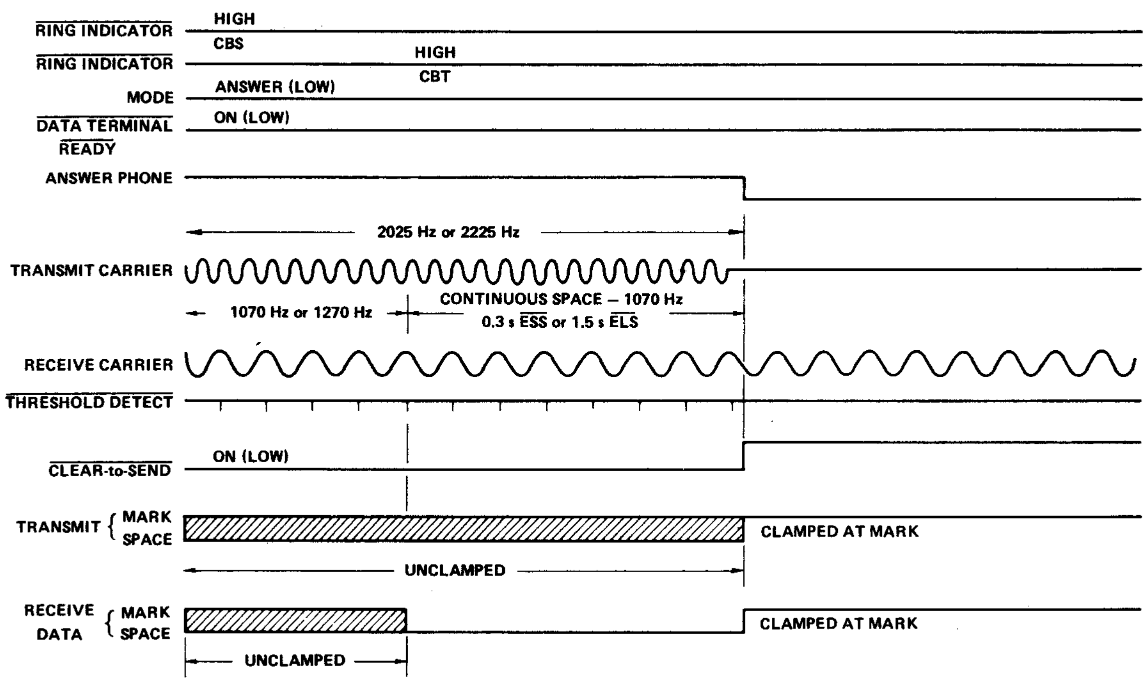


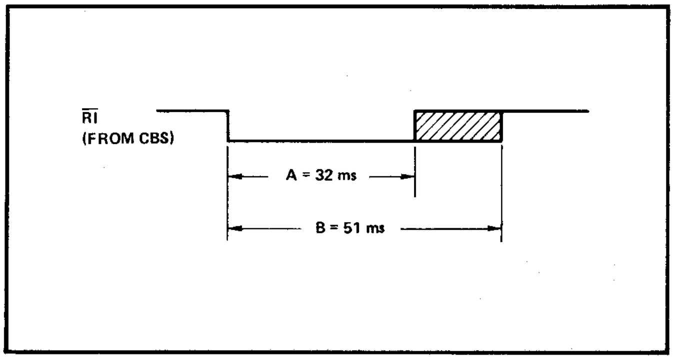
FIGURE 9 AUTOMATIC DISCONNECT – LONG OR SHORT SPACE

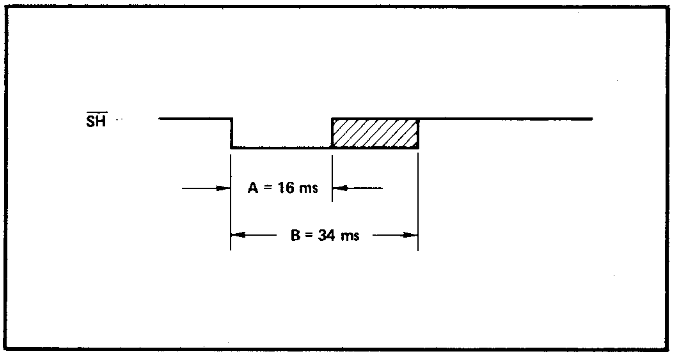
TABLE 1 ASYNCHRONOUS INPUT PULSE WIDTH AND OUTPUT DELAY VARIATIONS

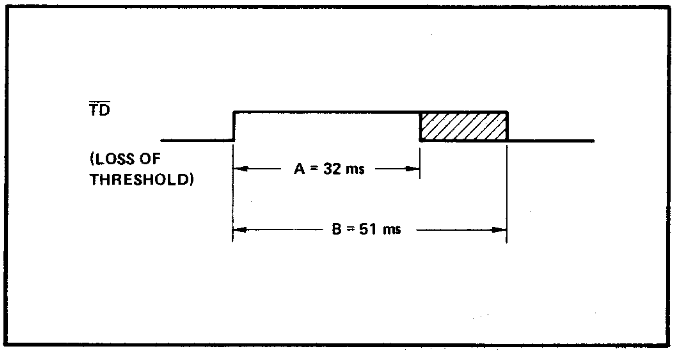
Due to the asynchronous nature of the input signals with respect to the circuit internal clock, a delay variation or input pulse width requirement will exist. Time delay A is the maximum time for which no response will occur. Time delay B is the minimum time required to guarantee an input response. Input signal widths in the cross hatched region (i.e., greater than A but less than B) may or may not be recognized as valid.

For output delays, time A is the minimum delay before an output will respond. Time B is the maximum delay for an output to respond. Output signal response may or may not occur in the cross hatched region (i.e., greater than A but less than B).

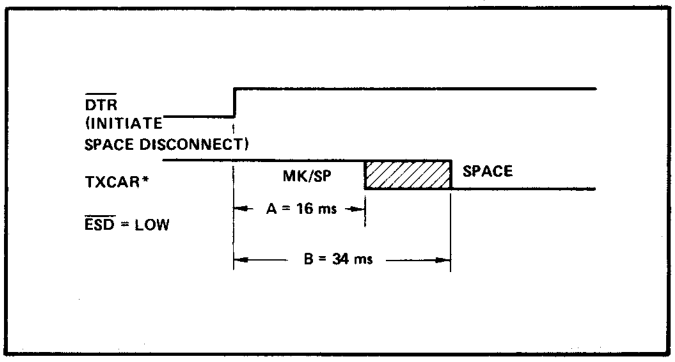
INPUT PULSES

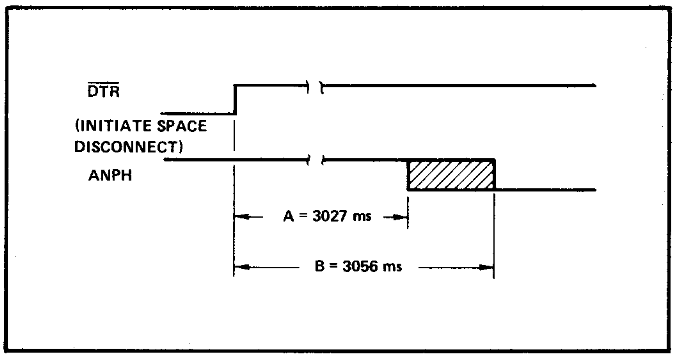


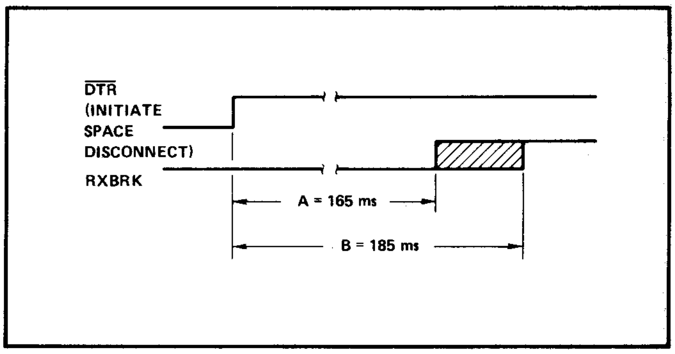




OUTPUT DELAYS



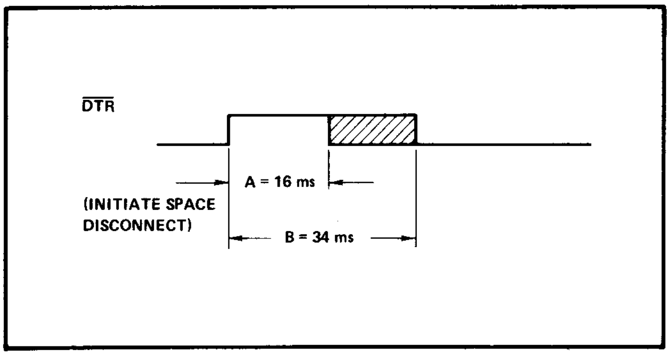


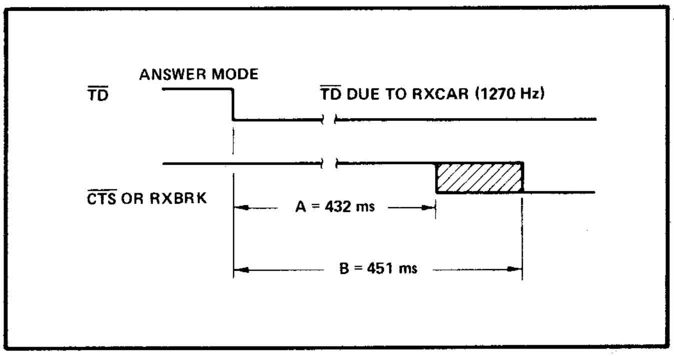


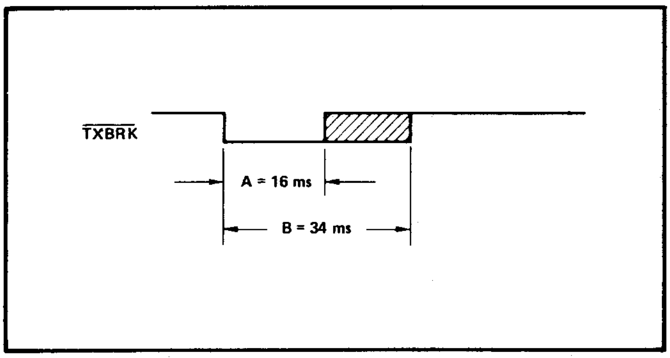
*DIGITAL REPRESENTATION

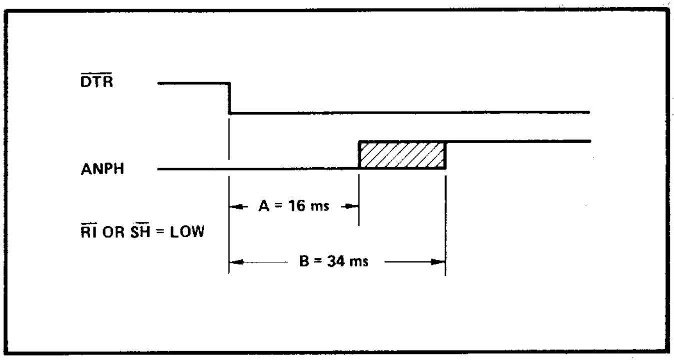
TABLE 1 OUTPUT DELAY VARIATIONS (continued)

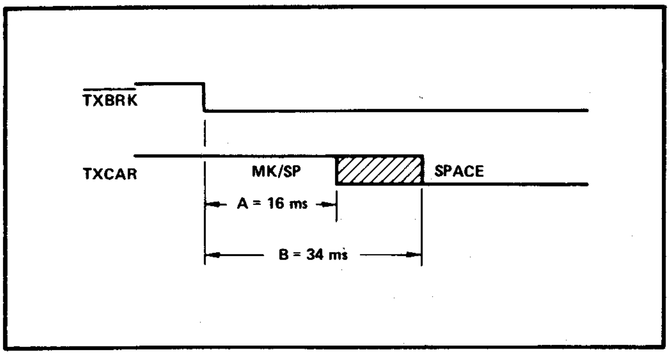
INPUT PULSES / **OUTPUT DELAYS**

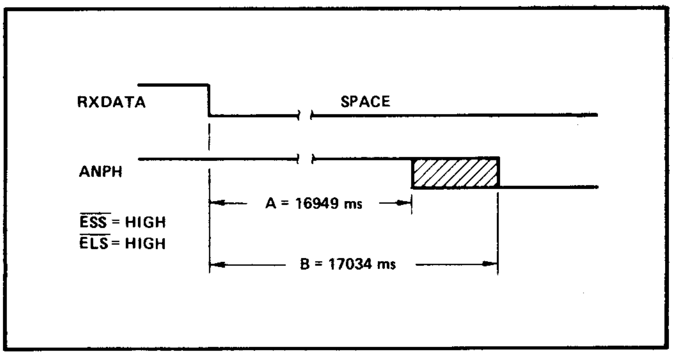


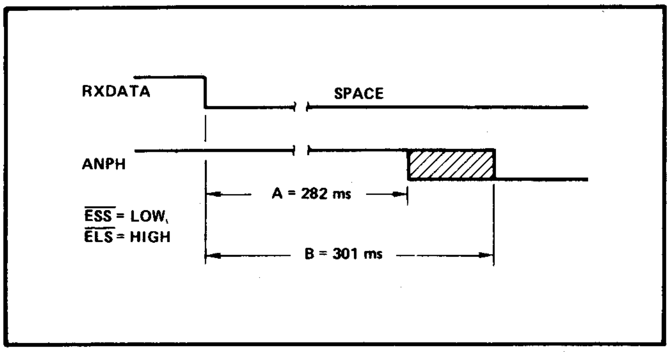












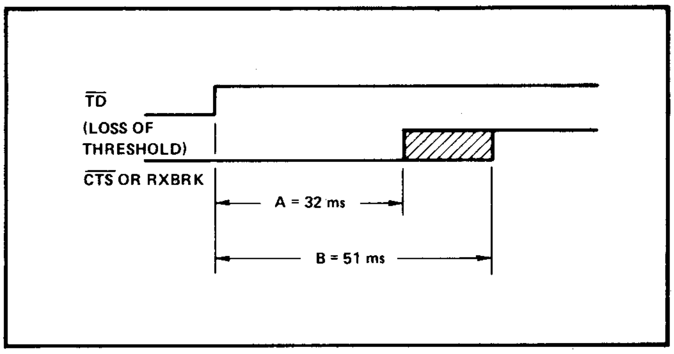
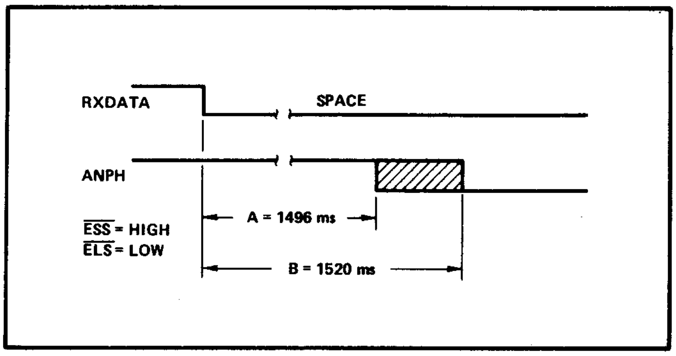
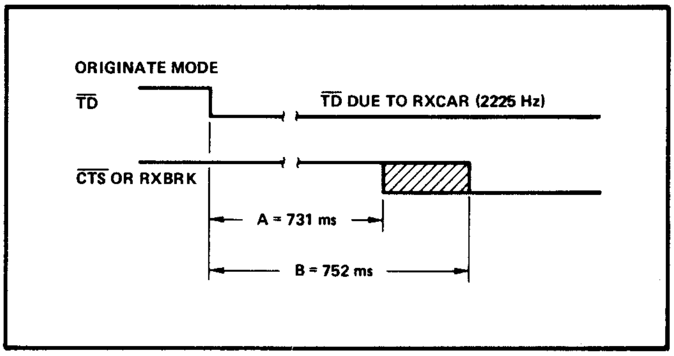
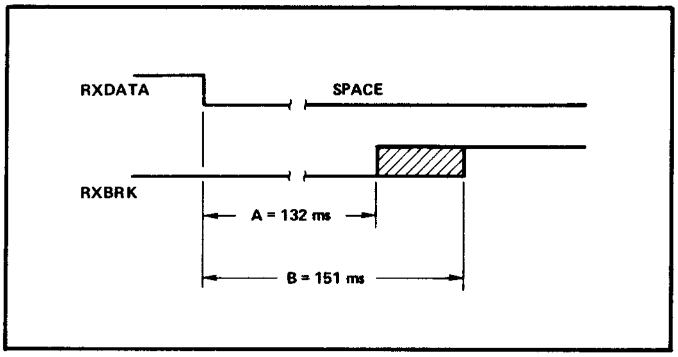


TABLE 1 OUTPUT DELAY VARIATIONS (Continued)

INPUT PULSES | **OUTPUT DELAYS**







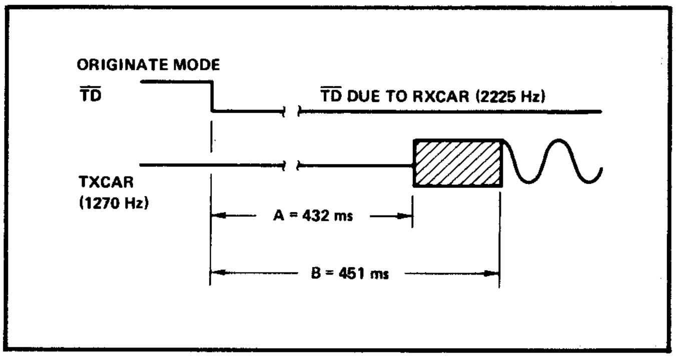


TABLE 2 TRANSMIT BREAK AND DISCONNECT DELAYS

Function Description	Min	Max	Unit
$\overline{TXBRK}$ (Space Duration)	232	235	ms
Space Disconnect (Space Duration) ($\overline{DTR}$ = High, $\overline{ESD}$ and $\overline{TD}$ = Low)	3010	3023	ms
Loss of Carrier Disconnect (Measured from positive edge of $\overline{CTS}$ to negative edge of ANPH, with $\overline{RI}$, $\overline{SH}$, and $\overline{TD}$ = High)	16965	17034	ms
Override Disconnect (Measured from positive edge of $\overline{RI}$ or $\overline{SH}$ to negative edge of ANPH with $\overline{TD}$ = High)	16916	17101	ms

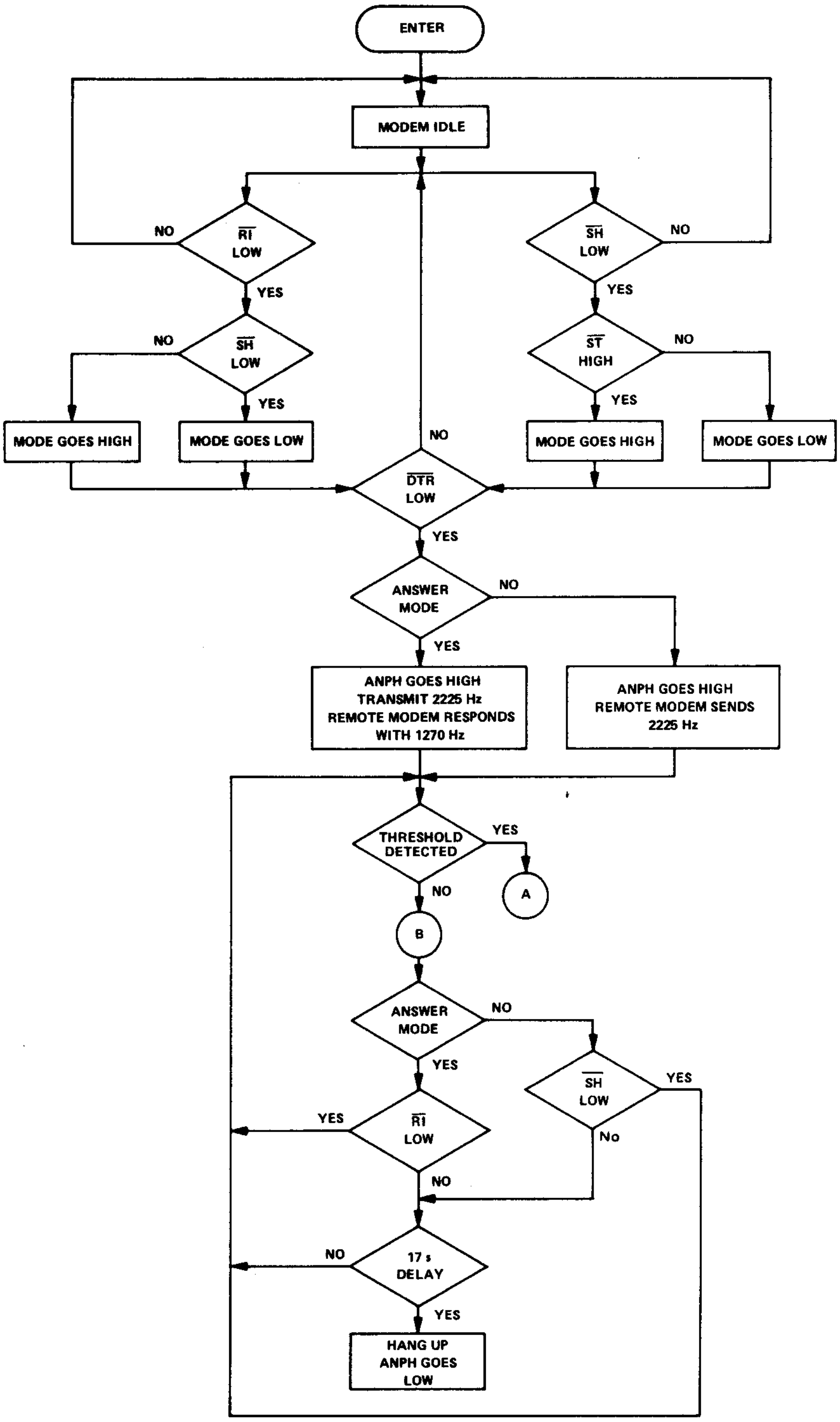
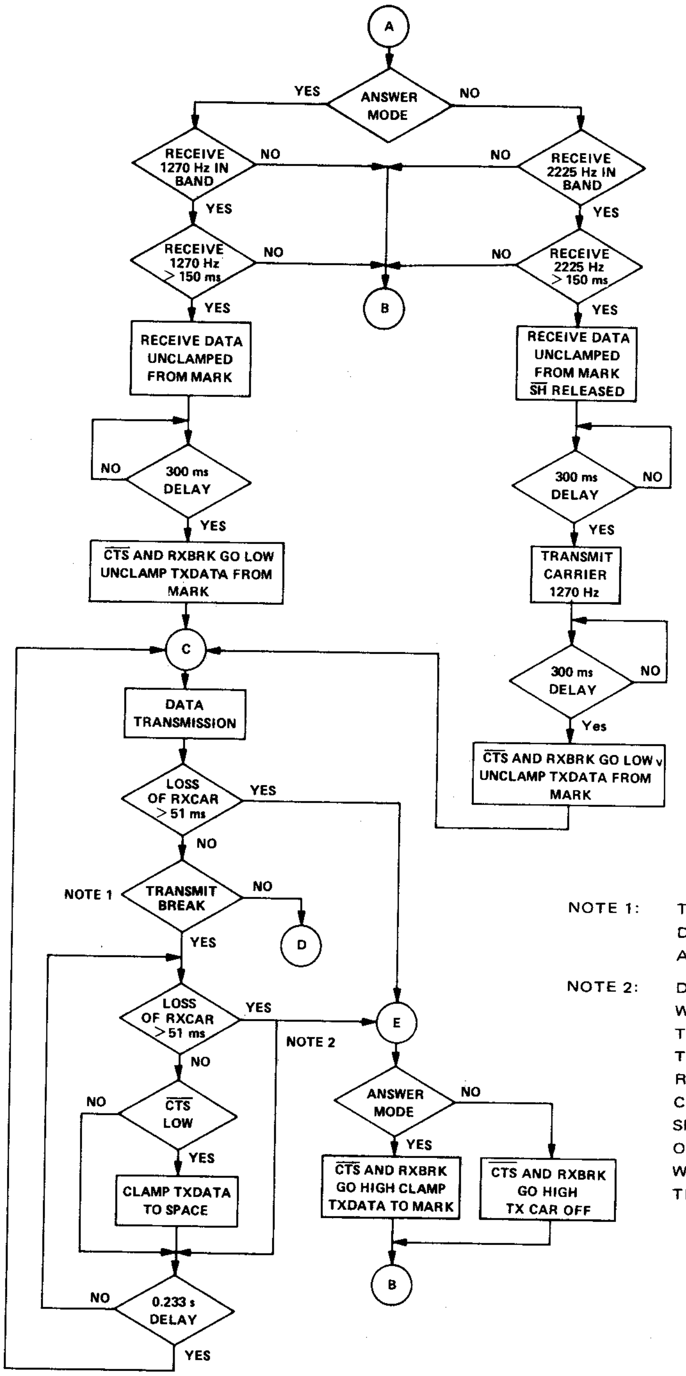
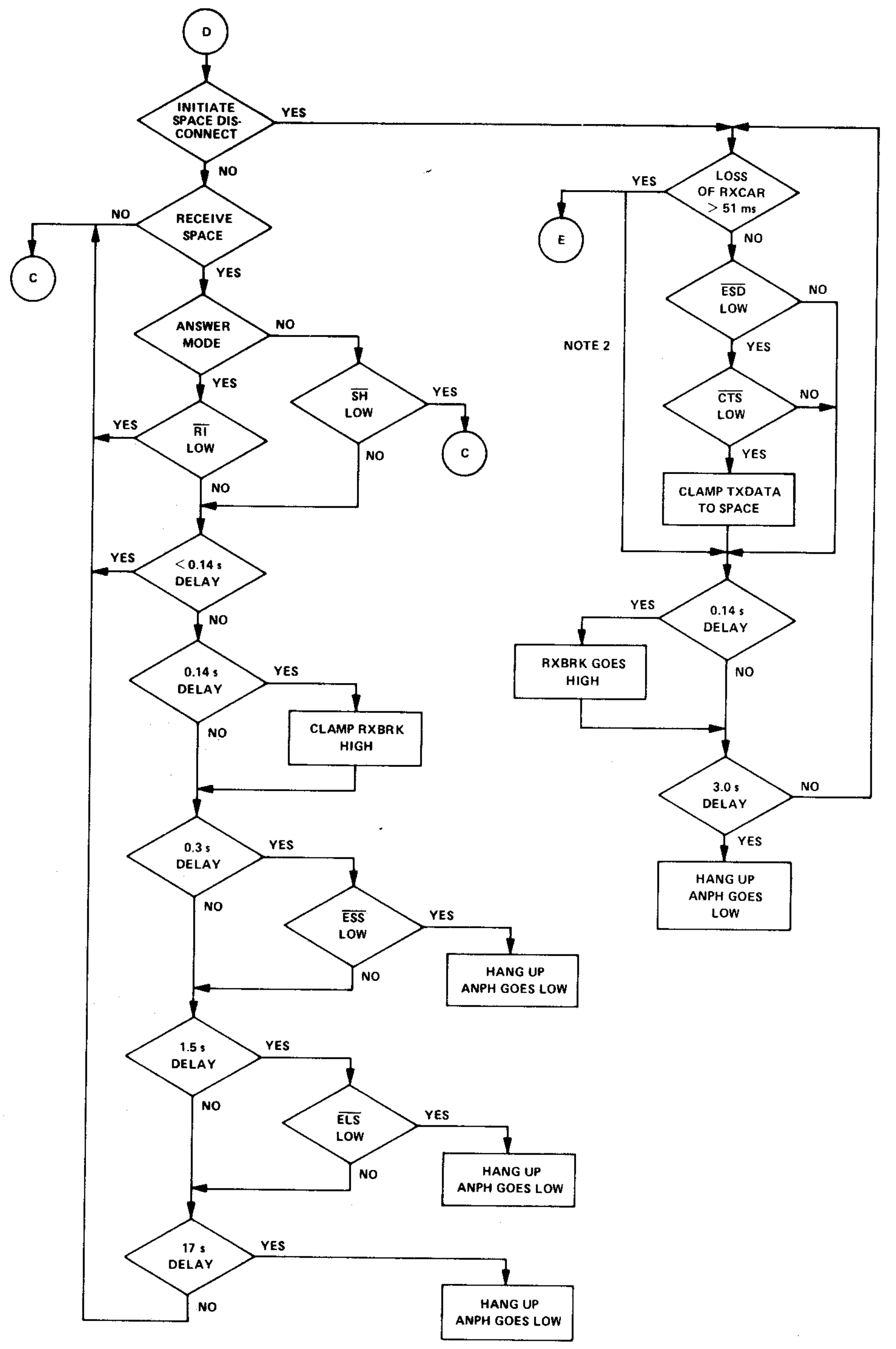


FIGURE 10 FLOW DIAGRAM



NOTE 1: TRANSMIT BREAK, INITIATE SPACE DISCONNECT, AND RECEIVE SPACE ARE MUTUALLY EXCLUSIVE EVENTS.

NOTE 2: DUE TO LOSS OF RXCAR, THE MODEN WILL CLAMP TXDATA TO A MARK IN THE ANSWER MODE AND WILL TURN OFF TXCAR IN THE ORIGINATE MODE. IF RXCAR IS DETECTED BEFORE A COMPLETION OF TXBRK OR INITIATE SPACE DISCONNECT, NORMAL OPERATION OF TXBRK OR INITIATE SPACE DISCONNECT WILL CONTINUE UNTIL COMPLETION OF THEIR RESPECTIVE TIME DELAYS.

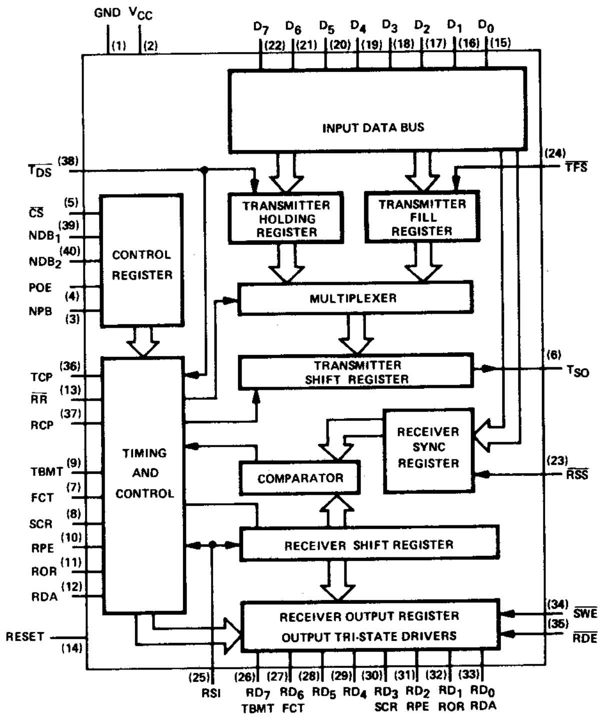

D
INITIATE SPACE DIS-CONNECT
YES
NO
RECEIVE SPACE
NO
C
YES
ANSWER MODE
NO
YES
SH LOW
YES
C
NO
RI LOW
YES
NO
< 0.14 s DELAY
YES
NO
0.14 s DELAY
YES
CLAMP RXBRK HIGH
NO
0.3 s DELAY
YES
ESS LOW
YES
HANG UP ANPH GOES LOW
NO
NO
1.5 s DELAY
YES
ELS LOW
YES
HANG UP ANPH GOES LOW
NO
NO
17 s DELAY
YES
HANG UP ANPH GOES LOW
NO
LOSS OF RXCAR > 51 ms
YES
E
NO
ESD LOW
NO
YES
NOTE 2
CTS LOW
NO
YES
CLAMP TXDATA TO SPACE
0.14 s DELAY
YES
RXBRK GOES HIGH
NO
3.0 s DELAY
NO
YES
HANG UP ANPH GOES LOW

S2350

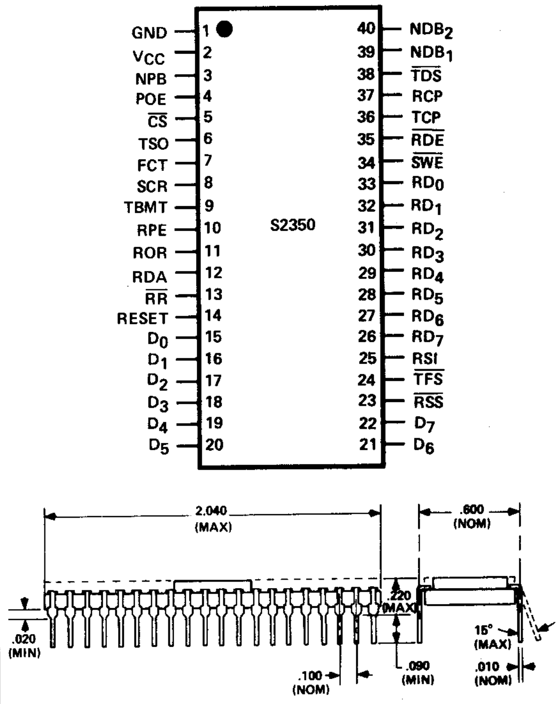
UNIVERSAL SYNCHRONOUS
RECEIVER/TRANSMITTER (USRT)

AMERICAN MICROSYSTEMS, INC.

ADVANCED PRODUCT DESCRIPTION



BLOCK DIAGRAM



PIN/PACKAGE CONFIGURATION

FEATURES

- 500 KHz Data Rates
- Internal Sync Detection
- Fill Character Register
- Double Buffered Input/Output
- Bus Oriented Outputs
- 5–8 Bit Characters
- Odd/Even or No Parity
- Error Status Flags
- Single Power Supply (+5v)
- Input/Output TTL Compatible

FUNCTIONAL DESCRIPTION

The S2350 Universal Synchronous Receiver Transmitter (USRT) is a single chip MOS/LSI device that totally replaces the serial to parallel and parallel to serial conversion logic required to interface a word parallel controller or data terminal to a bit-serial, synchronous communication network.

The USRT consists of separate receiver and transmitter sections with independent clocks, data lines and status. Common with the transmitter and receiver are word length and parity mode. Data is transmitted and received in a NRZ format at a rate equal to the respective input clock frequency.

Data messages are transmitted as a contiguous character stream, bit synchronous with respect to a clock and character synchronous with respect to framing or "sync" characters initializing each message. The USRT receiver compares the contents of the internal Receiver Sync Register with the incoming data stream in a bit transparent mode. When a compare is made, the receiver becomes character synchronous formatting a 5, 6, 7, or 8 bit character for output each character time. The receiver has an output buffer register allowing a full character time to transfer the data out. The receiver status outputs indicate received data available (RDA), receiver overrun (ROR), receive parity error (RPE) and sync character

received (SCR). Status bits are available on individual output lines and can also be multiplexed onto the output data lines for bus organized systems. The data lines have tri-state outputs.

The USRT transmitter outputs 5, 6, 7, or 8 bit characters with correct parity at the transmitter serial output (TSO). The transmitter is buffered to allow a full character time to respond to a transmitter buffer empty (TBMT) request for data. Data is transmitted in a NRZ format changing on the positive transition of the transmitter clock (TCP). The character in the transmitter fill register is inserted into the data message if a data character is not loaded into the transmitter after a TBMT request.

TYPICAL APPLICATIONS

- Computer Peripherals
- Communication Concentrators
- Integrated Modems
- High Speed Terminals
- Time Division Multiplexing
- Industrial Data Transmission

ABSOLUTE MAXIMUM RATINGS

Ambient temperature under bias	0°C to + 70°C
Storage temperature	–65°C to +150°C
Positive voltage on any pin with respect to GROUND	+7 volt
Negative voltage on any pin with respect to GROUND	–0.5 volt
Power dissipation	0.75 watt

DC (STATIC) CHARACTERISTICS*
V_{CC} = +5V ±5V ±5%, T_A = 25°C unless otherwise noted.

Symbol	Parameter	Min.	Max.	Unit	Condition
V_{IH}	Input High Voltage	2.0	V_{CC}	Volt	
V_{IL}	Input Low Voltage	- 0.5	+0.8	Volt	
I_{IL}	Input Leakage Current		10	μa	V_{IN} = 0TO V_{CC} Volts
V_{OH}	Output High Voltage	2.4		Volts	I_{OH} = –100μa
V_{OL}	Output Low Voltage		+0.4	Volts	I_{OL} = 1.6ma
C_{IN}	Input Capacitance		10	pf	V_{IN} = 0 Volt, f = 1.0 MHZ
C_{OUT}	Output Capacitance		12	pf	V_{IN} = 0 Volt, f = 1.0 MHZ
I_{CC}	V_{CC} Supply Current		100	ma	No Load

*Electrical characteristics included in this advanced product description are objective specifications and may be subject to change.

AC (DYNAMIC) CHARACTERISTICS
V_{CC} = +5V ±5%, T_A = 25°C unless otherwise noted.

Symbol	Parameter	Min.	Max.	Unit	Condition
TCP, RCP	Clock Frequency	DC	500	KHz	

Input Pulse Widths

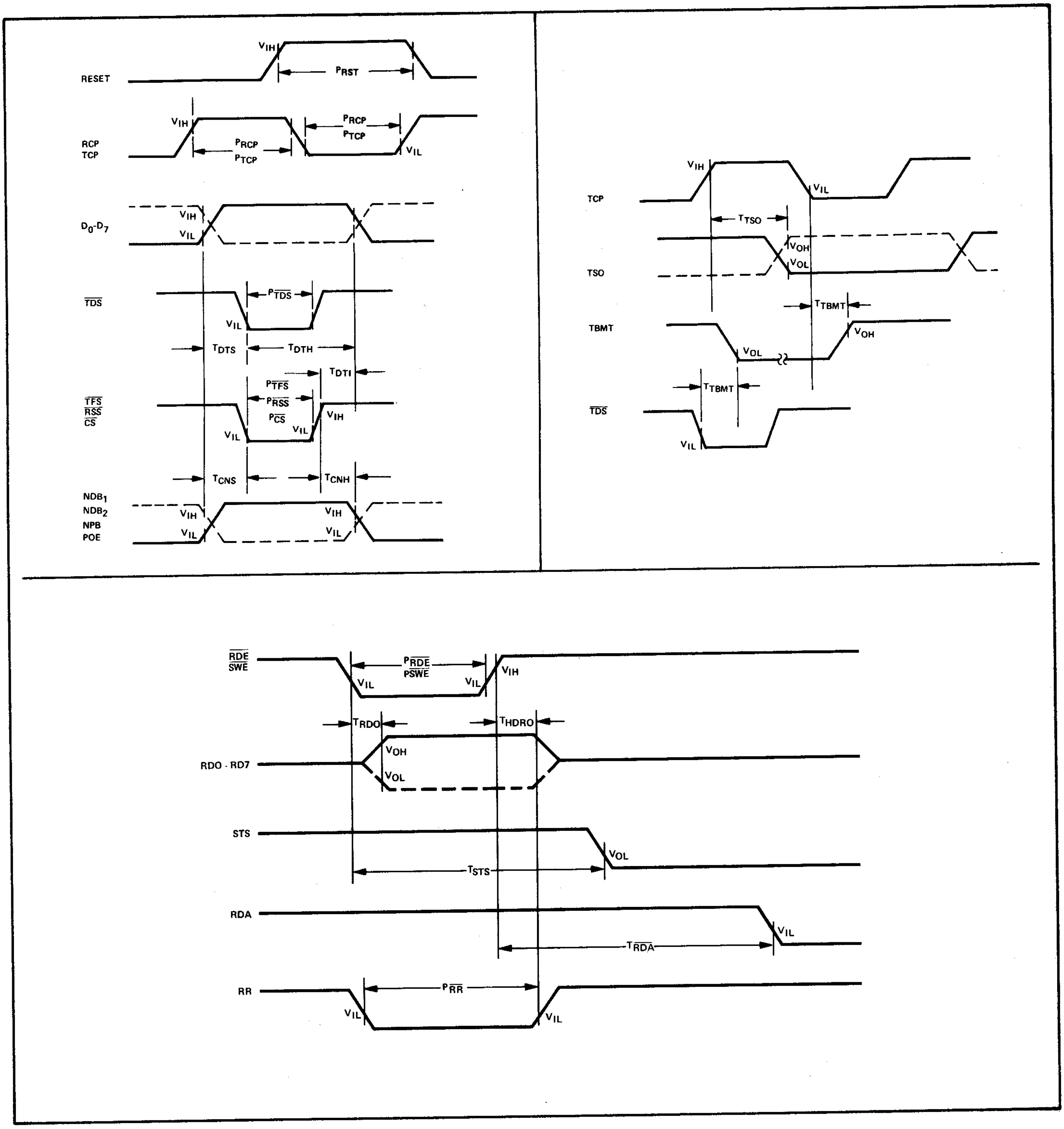
P_{TCP}	Transmit Clock	900		nsec	C_L = 20pf
P_{RCP}	Receive Clock	900		nsec	1TTL Load
P_{RST}	Reset	500		nsec	
$P_{\overline{TDS}}$	Transmit Data Strobe	200		nsec	
$P_{\overline{TFS}}$	Transmit Fill Strobe	200		nsec	
$P_{\overline{RSS}}$	Receive Sync Strobe	200		nsec	
$P_{\overline{CS}}$	Control Strobe	200		nsec	
$P_{\overline{RDE}}$	Receive Data Enable	400		nsec	Note 1
$P_{\overline{SWE}}$	Status Word Enable	400		nsec	Note 1
$P_{\overline{RR}}$	Receiver Restart	500		nsec	

Switching Characteristics

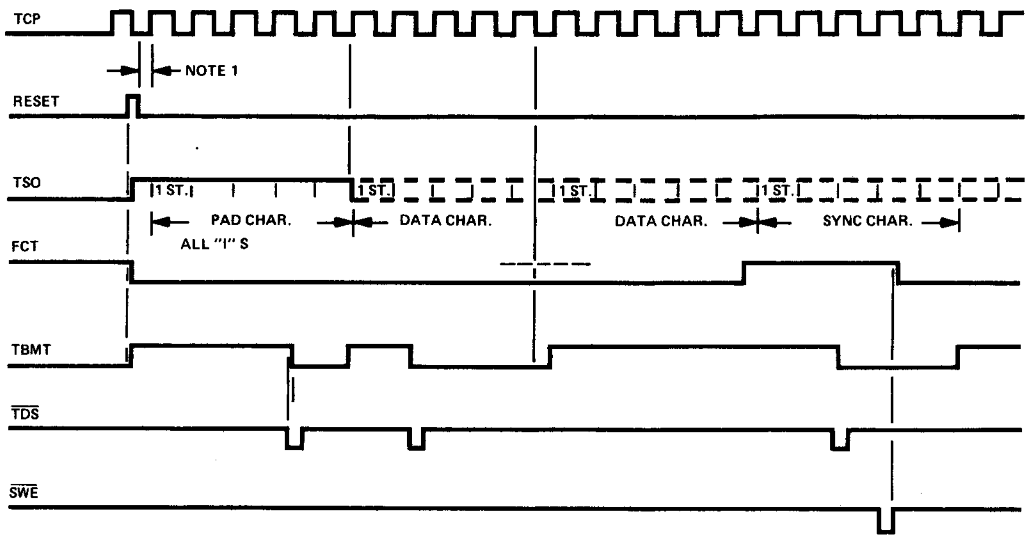
T_{TSO}	Delay, TCP Clock to Serial Data Out		700	nsec	
T_{TBMT}	Delay, TCP Clock to TBMT Output		1.4	μsec	
T_{TBMT}	Delay, $\overline{TDS}$ to TBMT		700	nsec	
T_{STS}	Delay, $\overline{SWE}$ to Status Reset		700	nsec	
T_{RDO}	Delay, $\overline{SWE}$, $\overline{RDE}$ to Data Outputs		400	nsec	1TTL Load
T_{HRDO}	Hold Time $\overline{SWE}$, $\overline{RDE}$ to Off State		400	nsec	C_L = 130 pf
T_{DTS}	Data Set Up Time $\overline{TDS}$, $\overline{TFS}$, $\overline{RSS}$, $\overline{CS}$	0		nsec	
T_{DTH}	Data Hold Time $\overline{TDS}$	700		nsec	
T_{DTI}	Data Hold Time $\overline{TFS}$, $\overline{RSS}$	200		nsec	
T_{CNS}	Control Set Up Time NDB1, NDB2, NPB, POE	0		nsec	
T_{CNH}	Control Hold Time NDB1, NDB2, NPB, POE	200		nsec	
T_{RDA}	Delay $\overline{RDE}$ to $\overline{RDA}$ Output	700		nsec	

NOTE 1: Required to reset status and flags.

TIMING WAVEFORMS

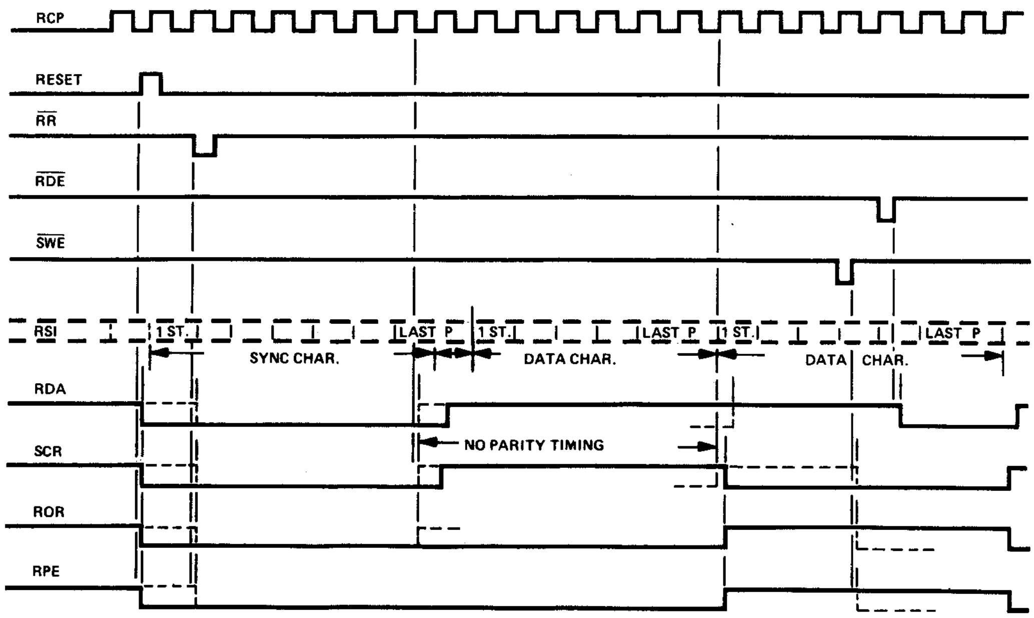


TRANSMITTER TIMING DIAGRAM



NOTE 1 DATA TRANSMISSION WILL START ON THE FIRST LOW TO HIGH TRANSITION OF TCP AFTER RESET IS LOW. THE INITIAL RESET PULSE SHOULD NOT OCCUR UNTIL 100 MICROSECONDS AFTER POWER IS APPLIED.

RECEIVER TIMING DIAGRAM



PIN DEFINITIONS

Pin	Label	Function
(1)	GND	Ground
(2)	V_{CC}	+5 VOLTS ±5%
(14)	RESET	MASTER RESET A V_{IH} initializes both the receiver and transmitter. The Transmitter Shift Register is set to output a character of all logic 1's. FCT is reset to V_{OL} and TBMT set to V_{OH} indicating the Transmitter Holding Register is empty. The receiver status is initialized to a V_{OL} on RPE, SCR, and RDA. The sync character detect logic is inhibited until a RR pulse is received.
(15) (16) (17) (18) (19) (20) (21) (22)	D0 D1 D2 D3 D4 D5 D6 D7	DATA INPUTS Data on the eight data lines are loaded into the Transmitter Holding Register by $\overline{TDS}$, the Transmitter Fill Register by $\overline{TFS}$, and the Receiver Sync Register by $\overline{RSS}$. The character is right justified with the LSB at D0. For word lengths less than 8 bits, the unused inputs are ignored. Data transmission is LSB first.
(38)	$\overline{TDS}$	TRANSMIT DATA STROBE A V_{IL} loads data on D0-D7 into the Transmitter Holding Register and resets TBMT to a V_{OL}.
(24)	$\overline{TFS}$	TRAMSMIT FILL STROBE A V_{IL} loads data on D0-D7 into the Transmitter Fill Register. The character in the Transmitter Fill Register is transmitted whenever a new character is not loaded in the allotted time.
(23)	$\overline{RSS}$	RECEIVER SYNC STROBE A V_{IL} loads data on D0-D7 into the Receiver Sync Register. SCR is set to V_{OH} whenever data in the Receiver Shift Register compares with the character in the Receiver Sync Register.
(9)	TBMT	TRANSMIT BUFFER EMPTY A V_{OH} indicates the data in the Transmitter Holding Register has been transferred to the Transmitter Shift Register and new data may be loaded. TBMT is reset to V_{OL} by a V_{IL} on $\overline{TDS}$. A V_{IH} on RESET sets TBMT to a V_{OH}. TBMT is also multiplexed onto the RD7 output (26) when $\overline{SWE}$ is at V_{IL} and $\overline{RDE}$ is at V_{IH}.
(6)	TSO	TRANSMITTER SERIAL OUTPUT Data entered on D0-D7 are transmitted serially, least significant bit first, on TSO at a rate equal to the Transmit Clock frequency, TCP. Source of the data to the transmitter shift register is the Transmitter Holding Register or Transmitter Fill Register.
(36)	TCP	TRANSMIT CLOCK Data is transmitted on TSO at the frequency of the TCP input in a NRZ format. A new data bit is started on each negative to positive transition (V_{IL} to V_{IH}) of TCP.

Pin	Label	Function
(26) (27) (28) (29) (30) (31) (32) (33)	RD7 RD6 RD5 RD4 RD3 RD2 RD1 RD0	RECEIVED DATA OUTPUTS RDO-RD7 contain data from the Receiver Output Register or selective status conditions depending on the state of $\overline{SWE}$ and $\overline{RDE}$ per the following table:

(34)	(35)	(33)	(32)	(31)	(30)	(39)	(28)	(27)	(26)
$\overline{SWE}$	$\overline{RDE}$	RD0	RD1	RD2	RD3	RD4	RD5	RD6	RD7
V_{IL}	V_{IL}	X	X	X	X	X	X	X	X
V_{IL}	V_{IH}	RDA	ROR	RPE	SCR	V_{OL}	V_{OL}	FCT	TBMT
V_{IH}	V_{IL}	DB0	DB1	DB2	DB3	DB4	DB5	DB6	DB7
V_{IH}	V_{IH}	X	X	X	X	X	X	X	X

X Output is in the OFF or Tri-State condition
DB0 LSB of Receiver Output Register
DB7 MSB of Receiver Output Register
The two unused outputs are held at V_{OL} in the output status condition.

Pin	Label	Function
(35)	$\overline{RDE}$	RECEIVE DATA ENABLE A V_{IL} enables the data in the Receiver Output Register onto the output data lines RD0–RD7. The trailing edge (V_{IL} to V_{IH} transition) of $\overline{RDE}$ resets RDA to the V_{OL} condition.
(7)	FCT	FILL CHARACTER TRANSMITTED A V_{OH} on FCT indicates data from the Transmitter Fill Register has been transferred to the Transmitter Shift Register. FCT is reset to V_{OL} when data is transferred from the Transmitter Holding Register to the Transmitter Shift Register, or on the trailing edge (V_{IL} to V_{IH}) of the $\overline{SWE}$ pulse, or when RESET is V_{IH}. FCT is multiplexed onto the RD6 output (27) when $\overline{SWE}$ is at V_{IL} and $\overline{RDE}$ is at V_{IH}.
(25)	RSI	RECEIVER SERIAL INPUT Serial data is clocked into the Receiver Shift Register, least significant bit first, on RSI at a rate equal to the Receive Clock frequency RCP.
(37)	RCP	RECEIVE CLOCK Data is transferred from RSI input to the Receiver Shift Register at the frequency of the RCP input. Each data bit is entered on the positive to negative transition (V_{IH} to V_{IL}) of RCP.

Pin	Label	Function
(12)	RDA	RECEIVED DATA AVAILABLE A V_{OH} indicates a character has been transferred from the Receiver Shift Register to the Receiver Output Register. RDA is reset to V_{OL} on the trailing edge (V_{IL} to V_{IH} transition) of $\overline{RDE}$, by a V_{IL} on $\overline{RR}$ or a V_{IH} on RESET. RDA is multiplexed onto the RD0 output (33) when $\overline{SWE}$ is V_{IL} and $\overline{RDE}$ is V_{IH}.
(8)	SCR	SYNC CHARACTER RECEIVED A V_{OH} indicates the data in the Receiver Shift Register is identical to the data in the Receiver Sync Register. SCR is reset to a V_{OL} when the character in the Receiver Shift Register does not compare to the Receiver Sync Register, on the trailing edge (V_{IL} to V_{IH} transition) of $\overline{SWE}$, by a V_{IL} on $\overline{RR}$ or a V_{IH} on RESET. SCR is multiplexed onto the RD3 output (30) when $\overline{SWE}$ is a V_{IL} and $\overline{RDE}$ is V_{IH}.
(34)	$\overline{SWE}$	STATUS WORD ENABLE A V_{IL} enables the internal status conditions onto the output data lines RD0–RD7. The trailing edge of $\overline{SWE}$ pulse resets FCT, ROR, RPE, and SCR to V_{OL}.
(11)	ROR	RECEIVER OVERRUN A V_{OH} indicates data has been transferred from the Receiver Shift Register to the Receiver Output Register when RDA was still set to V_{OH}. The last data in the Output Register is lost. ROR is reset by the trailing edge (V_{IL} to V_{IH}) of $\overline{SWE}$, a V_{IL} on $\overline{RR}$, a V_{IH} on RESET or a V_{OL} to V_{OH} transition of RDA. ROR is multiplexed onto the RD1 output (32) when $\overline{SWE}$ is V_{IL} and $\overline{RDE}$ is V_{IH}.
(10)	RPE	RECEIVER PARITY ERROR A V_{OH} indicates the accumulated parity on the received character transferred to the Output Register does not agree with the parity selected by POE. RPE is reset with the next received character with correct parity, the trailing edge (V_{IL} to V_{IH}) of $\overline{SWE}$, a V_{IL} on $\overline{RR}$ or a V_{IH} on RESET. RPE is multiplexed onto the RD2 output (31) when $\overline{SWE}$ is V_{IL} and $\overline{RDE}$ is V_{IH}.
(13)	$\overline{RR}$	RECEIVER RESTART A V_{IL} resets the receiver section by clearing the status RDA, SCR, ROR, and RPE to V_{OL}. The trailing edge of $\overline{RR}$ (V_{IL} to V_{IH}) also puts the receiver in a bit transparent mode to search for a comparison, each bit time, between the contents of the Receiver Shift Register and the Receiver Sync Register. The number of data bits per character for the comparison is set by NDB1 and NDB2. After a compare is made SCR is set to V_{OH}, the sync character is transferred to the Receiver Output Register, and the receiver enters a word synchronous mode framing an input character each word time. NOTE: Parity is not checked on the first sync character but is enabled for every succeeding character.

Pin	Label	Function
(39)	NDB1	NUMBER DATA BITS The number of Data Bits per character are determined by NDB1 and NDB2. The number of data bits does not include the parity bit.

NDB2	NDB1	CHARACTER LENGTH
V_{IL}	V_{IL}	5 Bits
V_{IL}	V_{IH}	6 Bits
V_{IH}	V_{IL}	7 Bits
V_{IH}	V_{IH}	8 Bits

For character lengths less than 8 bits, unused inputs are ignored and unused outputs are held to V_{OL}. Data is always right justified with D0 and RD0 being the least significant bits.

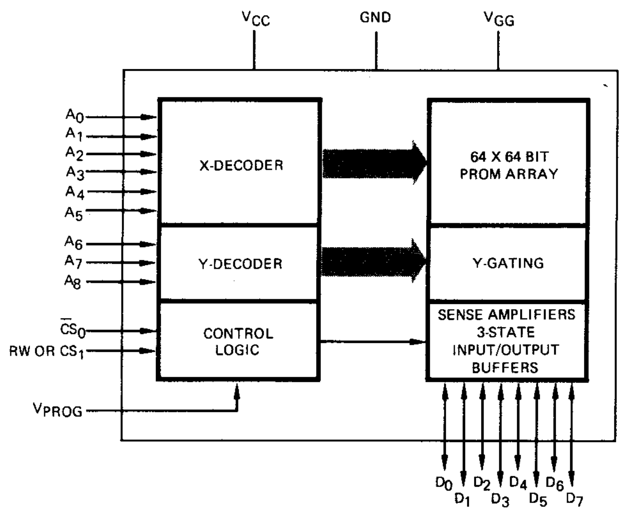
Pin	Label	Function
(3)	NPB	NO PARITY BIT A V_{IH} eliminates generation of a parity bit in the transmitter and checking of parity in the receiver. With parity disabled, the RPE status bit is held at V_{OL}.
(4)	POE	PARITY ODD/EVEN A V_{IH} directs both the transmitter and receiver to operate with even parity. A V_{IL} forces odd parity operation. NPB must be VIL for parity to be enabled.
(5)	$\overline{CS}$	CONTROL STROBE A V_{IL} loads the control inputs NDB1, NDB2, POE, and NPB into the Control Register. For static operation, $\overline{CS}$ can be tied directly to ground.

S6834

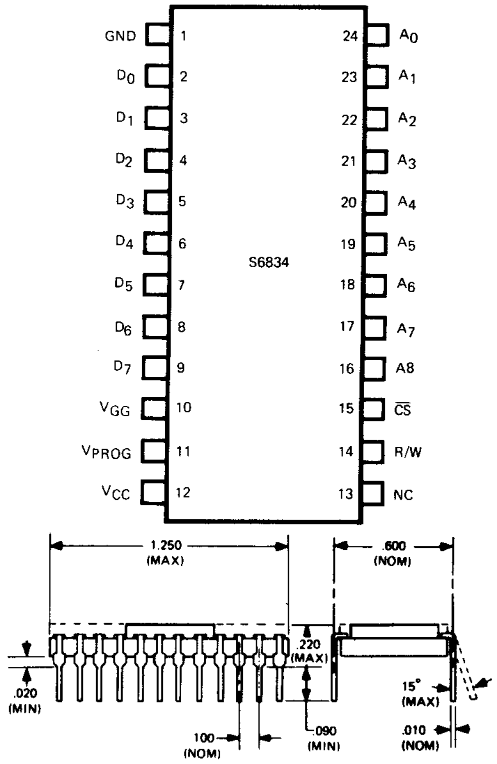
512 X 8 BIT
ERASEABLE AND
ELECTRICALLY REPROGRAMMABLE
READ ONLY MEMORY

AMERICAN MICROSYSTEMS, INC.

ADVANCED PRODUCT DESCRIPTION



BLOCK DIAGRAM



PIN/PACKAGE CONFIGURATION

FEATURES

- On-Board Programmability
- Fast Access Time – 500 ns Typ.
- Pin Configuration Similar to the S6830 1K x 8 Bit ROM
- High Speed Programming – Less than 1 Minute for all 4096 Bits
- Programmed with R/W, CS and V_{PROG} Pins
- Completely TTL Compatible – Excluding the V_{PROG} Pin
- Ultraviolet Light Erasable – Less than 10 Minutes
- Static Operation – No Clocks Required
- Three-State Data I/O
- Standard Power Supplies +5V and –12V
- Mature P-Chan Process

FUNCTIONAL DESCRIPTION

The S6834 is a high speed, static, 512 x 8 bit, eraseable and electrically programmable read only memory designed for use in bus-organized systems. Both input and output are TTL compatable during both read and write modes. Packaged in a 24 pin hermetically sealed dual in-line package the bit pattern can be erased by exposing the chip to an ultra-violet light source through the transparent lid, after which a new pattern can be written.

TYPICAL APPLICATIONS

- ROM Program Debugging
- Code Translation
- Microprogramming
- Look-up Tables
- Random Logic Replacement
- Programmable Waveforms
- Character Generation
- Electronic Keyboards

ABSOLUTE MAXIMUM RATINGS

Voltage on any pin relative to V_{SS} except the V_{PROG} pin	+0.3 to −20V
Voltage on the V_{PROG} pin relative to V_{SS}	+0.3 to −55V
Operating Temperature	0°C to +70°C
Storage Temperature (programmed)	−55°C to +85°C
Storage Temperature (unprogrammed)	−55°C to 150°C

NOTE: This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields, however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

DC (STATIC) CHARACTERISTICS (V_{CC} = +5.0V ± 5%, V_{GG} = −12.0V ± 5% T_A = 0 – 70°C unless otherwise noted).

SYMBOL	CHARACTERISTIC	MIN	MAX	UNIT
V_{IL}	INPUT VOLTAGE LOW		0.8	V
V_{IH}	INPUT VOLTAGE HIGH	V_{CC} −2.25	V_{CC} to .3	V
V_{OL}	OUTPUT VOLTAGE LOW I_{OL} = 1.6 ma		0.4	V
V_{OH}	OUTPUT VOLTAGE HIGH I_{OH} = 40 μa	2.4		V
I_{LI}	INPUT LEAKAGE CURRENT		20	μa
I_{LO}	OUTPUT LEAKAGE CURRENT CS = 5V		10	μa
I_{GG}	V_{GG} SUPPLY CURRENT		45	ma
I_{CC}	V_{CC} SUPPLY CURRENT		50	ma
P_D	POWER DISSIPATION		750	mw

NOTE: Program input V_{PROG} may be tied to V_{CC} during the Read.

AC (DYNAMIC) CHARACTERISTICS (Loading is as shown in Figure 1 unless otherwise noted).

SYMBOL	CHARACTERISTIC	MIN	MAX (6834)	MAX (6834−1)	UNIT
T_{ACC}	ACCESS TIME		575	750	ns
T_{CO}	CHIP SELECT TO OUTPUT DELAY		300	400	ns
T_{DD}	CHIP DESELECT TO OUTPUT DELAY		250	325	ns

FIGURE 1 — TEST CONDITIONS

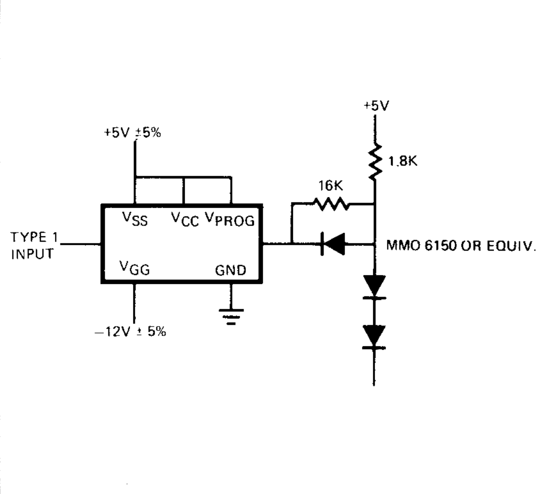
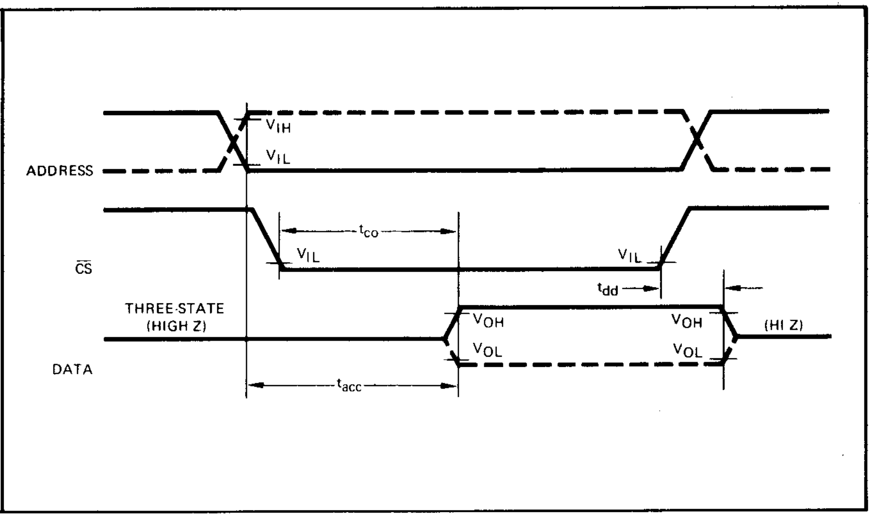


FIGURE 2 — READ CYCLE TIMING WAVEFORMS



PROGRAM CHARACTERISTICS (R/W G_{nd}, Program pulse rise and fall time (10% to 90%) are both at 1μs max).

SYMBOL	CHARACTERISTICS	MIN	MAX	UNIT
T_{AS}	ADDRESS SET UP TIME	10		μs
T_{CSS}	CHIP SELECT SET UP TIME	10		μs
T_{DS}	DATA SET UP TIME	10		μs
T_{AH}	ADDRESS HOLD TIME	10		μs
T_{CSH}	CHIP SELECT HOLD TIME	10		μs
T_{DH}	DATA HOLD TIME	10		μs
T_{PWL}	PROGRAM PULSE WIDTH LOW	3	5	ms
T_{PWH}	PROGRAM PULSE WIDTH HIGH	500		μs
V_{PROG}	PROGRAM AMPLITUDE	−55	−50	V
I_{PROG}	PROGRAM CURRENT		35	ma
T_{WS}	WRITE SET UP TIME	10		μs
T_{WH}	WRITE HOLD TIME	5		μs
T_{RS}	READ SET UP TIME	10		μs

FIGURE 3 —PROGRAMMING CYCLE TIMING WAVEFORMS

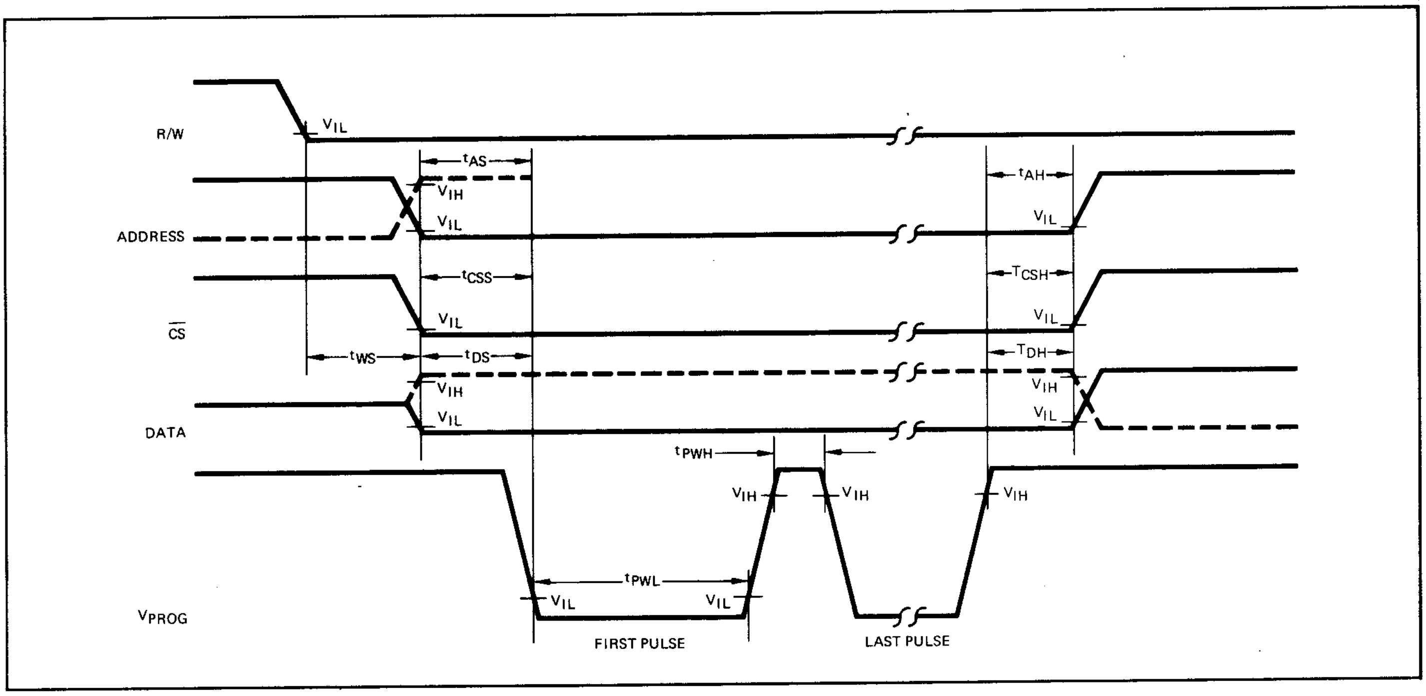
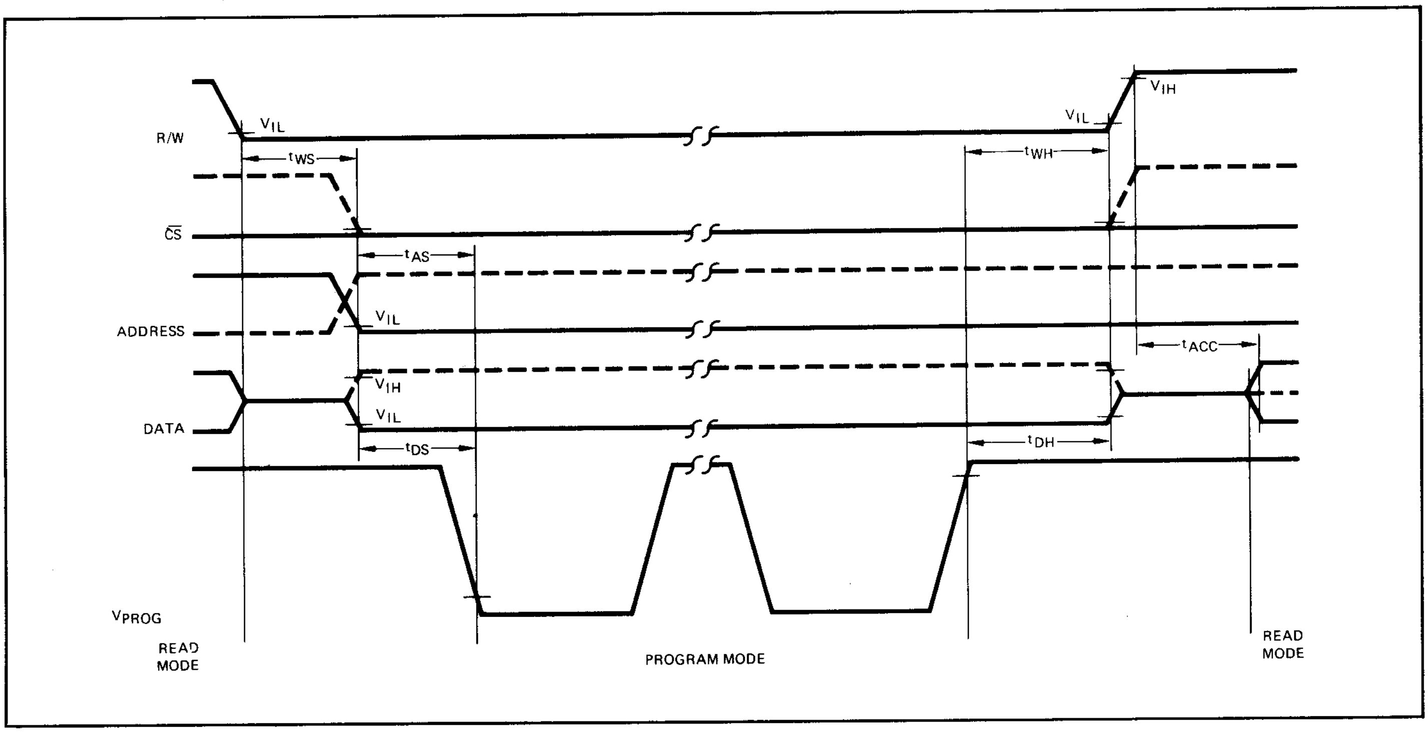


FIGURE 4 —READ/PROGRAM/READ CYCLE TIMING WAVEFORM



INTERFACE DESCRIPTION

Pin	Label	Function
(2) (3) (4) (5) (6) (7) (8) (9)	D0 D1 D2 D3 D4 D5 D6 D7	**Data Lines** – with the R/W line selected for Read (V_{IH}), the Data Lines (D0 through D7) are set to reflect the contents of the selected memory location. When the R/W line is set for Write (V_{IL}), the Data Lines are input to the addressed location of the 6834 when V_{PROG} is present. The Data Bus output drivers are three-state devices that remain in the high impedance (off) state whenever CS is in the V_{IH} state.
(14)	R/W	**Read/Write** – When this input line is set to V_{IH}, the device is in the Read mode, a low (V_{IL}) signal puts it into the Write mode.
(15)	CS	**Chip Select** – This input line must be set to V_{IL} for a Read or Write operation to be performed. When it is High (V_{IH}) the output data bus is set to a high-impedance three-state condition.
(11)	V_{PROG}	**Program** – In the Write mode, a programming pulse (–50V dc) at this input causes the data at the Data Lines to be stored in the selected address. This pin should be tied to V_{CC} for normal Read operations.
(24) (23) (22) (21) (20) (19) (18) (17) (16)	A0 A1 A2 A3 A4 A5 A6 A7 A8	**Address Lines** – These lines select the 8 bit word in memory for Read or Write operation.

CONTROL FUNCTION TRUTH TABLE

CS	R/W	V_{PROG}	MODE	OUTPUTS
0	0	V_{PROG}	Write	Active Data Inputs
0	1	V_{CC}	Read	Active
1	X	X	Standby	Floating

OPERATION

Initially, and after each erasure, all bits of the 6834 are in the logic "0" state (output 0 volts). Data is stored by selectively programming a logic "1" into the desired bit locations. The R/W input (pin 14) is used to select the desired mode of operation. When the R/W input is at logic "0" the chip is in the write enable mode of operation. The outputs (0_1 -0_8) are disabled (floating) with the corresponding pins becoming the data inputs ($0_1 \rightarrow D_{IN\ 1}$ etc.). The word address is selected in the same manner as in the read mode. Data to be programmed are presented 8 bits in parallel and after the address and data are set up a programming pulse (V_P −50 volts) is applied. V_{PROG} electrically writes the data into the memory array. Writing may be inhibited by deselecting the chip with the CS input at a logic "1" during the write cycle. This feature allows true "on board" programming in bus organized systems where the R/W and V_{PROG} inputs are common and the device to be programmed is selected by means of the chip select input as during read operations.

The amount of program energy required to insure memory retention may be defined as a function of the number of program pulses (N) times the program pulse width (t_{pw}) ($N \times t_{pw} \geqslant 60$ msec). This means if a 3 ms pulse is used, 20 program pulses are required, and if a 5 ms pulse is used 12 program pulses are required.

The read operation is accomplished by a logic "1" at the R/W input with the program input connected to V_{SS} potential. True data (data out = data in) is valid after the address is stable. The CS input will disable (float) the outputs when at a logic "1" to allow or tie capability.

Erasure is accomplished by exposing the array to a high intensity ultra-violet light source (such as, Ultra-Violet Products, Inc. Lamp Model S52 or UVS-54) for a period of 7 to 10 minutes. The clear optical lid should be approximately one inch away from the lamp tubes.

AMI

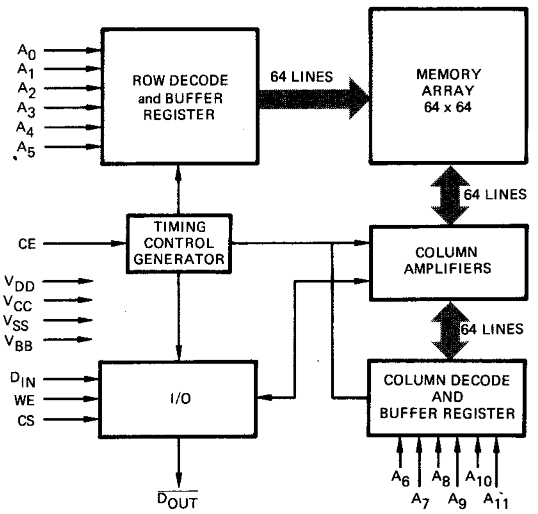
AMERICAN MICROSYSTEMS, INC.
3800 Homestead Road, Santa Clara, Ca. 95051/Telephone: (408) 246-0330, TWX: 910-338-0018

AMERICAN MICROSYSTEMS, INC.

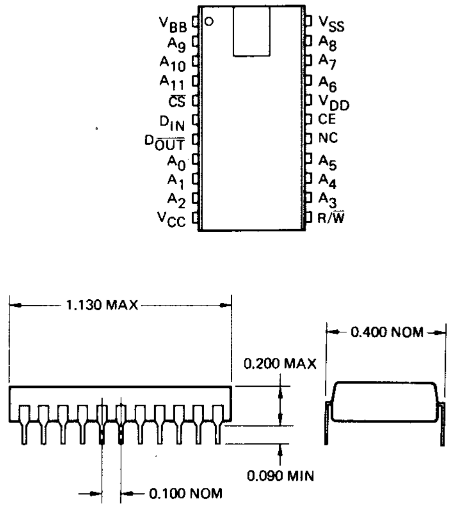
S4021-4

4096 X 1
RANDOM ACCESS MEMORY

ADVANCED PRODUCT DESCRIPTION



BLOCK DIAGRAM



PIN/PACKAGE CONFIGURATION

FEATURES

- Fast Access Time – 200ns (max)
- Fast Read or Write Cycle Time – 400ns (min)
- Fast Read Modify Write Cycle Time – 510ns (min)
- Low Power Dissipation – 360mw Operating (Typical) 1.8mw Standby (Typical)
- Output – Three State and TTL Compatible
- All Inputs TTL Compatible Except Chip Enable Clock
- Refresh Period – 2ms
- 22 Pin Dual-In-Line Package
- Pin Compatible With TMS 4060 and 2107B
- N-Channel Silicon Gate Technology
- One Transistor Per Cell Design
- Smallest 4096 Bit Dynamic RAM

FUNCTIONAL DESCRIPTION

The AMI S4021 series of dynamic read/write memories are designed for applications where high performance, low cost and large bit storage are desired in mainframe, add-on, and buffer memories and peripheral storage. The S4021 is a 4096 word by 1 bit array fabricated with selective oxidation N-Channel silicon gate technology. The S4021 uses a single transistor cell to achieve higher performance and smaller die size for low cost.

All addresses and control inputs are TTL compatible except for a single high voltage chip enable (CE) clock. All decoding is done on the chip using ratioless techniques to achieve low standby power dissipation.

The information read out is non-destructive (NDRO). Refresh of the entire memory is accomplished by performing one read cycle on each of the 64 row addresses (A_0 - A_5) every 2 ms.

TYPICAL APPLICATIONS

- Main Frame Memory
- Buffer Memory
- Add-on Memory
- Peripheral Storage
- Terminals
- Controllers, etc.

ABSOLUTE MAXIMUM RATINGS

Voltage on Any Pin Relative to Substrate . . . . -0.3V to + 20V
Operating Temperature Range . . . . 0°C to + 70°C
Storage Temperature . . . . -65° to + 150°C

COMMENT: Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification, is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. & OPERATING CHARACTERISTICS (T_A = 0° – 70°C, V_{DD} = +12V ± 5%, V_{CC} = +5V ± 5%, V_{BB} = -5V ± 5%, V_{SS} = 0V, unless noted)

Symbol	Parameters	Limits Min.	Limits Typ.	Limits Max.	Unit	Test Conditions
V_{IH}	Input High Voltage	2.4		V_{CC}+1	V	
V_{IL}	Input Low Voltage	-1.0		0.6	V	
V_{CEH}	CE, Input High Voltage	V_{DD} -0.6		V_{DD}+1	V	
V_{CEL}	CE, Input Low Voltage	-1.0		0.6	V	
V_{OH}	Output High Voltage	2.4		V_{CC}	V	I_{OH} = -2mA
V_{OL}	Output Low Voltage	V_{SS}		0.45	V	I_{OL} = 2.0mA
I_L	Input Leakage Current			10	μA	V_{IH} = 6.25V, V_{BB} = -5.25V
I_{CEL}	CE, Input Leakage Current			10	μA	V_{CEH} = 13.6V, V_{BB} = -5.25V
I_{IL01}	Output Leakage Current for High Impedence State			10	μA	V_{OH} = 5.25V, V_{BB} = -5.25V CS = 2.4V
I_{DDA}	Average V_{DD} to V_{SS} Current Active Mode		30	40	mA	RMW Cycle = 510ns T_{SB} = 130ns
I_{DD}	V_{DD} Supply Current During CE on		40		mA	
I_{DDS}	Average V_{DD} to V_{SS} Current, Standby Mode		150	500	μA	
I_{BB}	V_{BB} Supply Current		5	100	μA	
I_{CC}	V_{CC} Supply Current			10	μA	$\overline{CS}$ = 2.4V

A.C. & OPERATING CHARACTERISTICS ($T_A = 0°- 70°C$, $V_{DD} = +12V \pm 5\%$, $V_{CC} = +5V \pm 5\%$, $V_{BB} = -5V \pm 5\%$, $V_{SS} = 0V$, unless noted)

TABLE 1

Symbol	Parameter		Limit Min.	Limit Max.	Unit
t_{ACC}	Access time from Address			200	nsec
$t_{C(R)}$	Read Cycle Time		400		nsec
$t_{C(W)}$	Write Cycle Time		400		nsec
$t_{C(RMW)}$	Read Modify Write Cycle Time		510		nsec
t_{CE}	Chip Enable (CE) ON Time	Read Cycle	230		nsec
		Write Cycle	230		nsec
		RMW Cycle	340		nsec
t_{SB}	Chip Enable (CE)	OFF Time	130		nsec

NOTE: All timing with $t_T = 20$ nsec, Output load = One TTL gate and $C_{LOAD} = 50pF$

TABLE 2

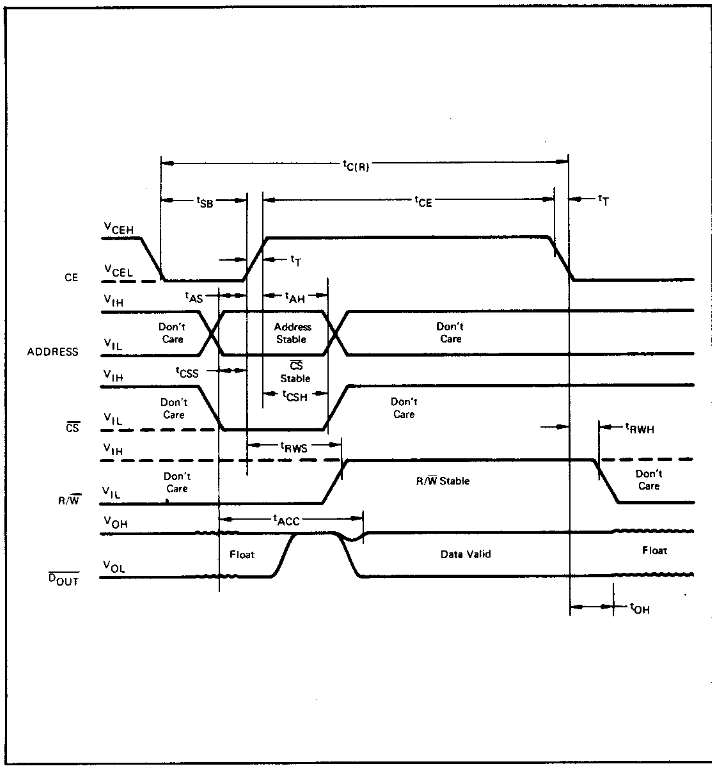
Symbol	Parameter		Limits Min.	Limits Max.	Units
t_{AS}	Address Set-Up Time		0		ns
t_{AH}	Address Hold Time		50		ns
t_{CSS}	Chip Select Set-Up Time		0		ns
t_{CSH}	Chip Select Hold Time		50		ns
t_{OH}	Output Hold Time		50		ns
t_{RWS}	Read Set-Up Time			50	ns
t_{RWH}	Read Hold Time		20		ns
t_{WPW}	Write Pulse Width		110		ns
t_{RWC}	Write Pulse Set-Up Time		140		ns
t_{WD}	Write Delay	Write Cycle	90		ns
		RMW Cycle	180		ns
t_{MOD}	Data Modify Time		0		ns
t_{DS}	Data-In Set-Up Time		0		ns
t_{DH}	Data-In Hold Time		40		ns
t_{OFF}	Output Off Time		20		ns
t_{OH}	Output Hold Time		50		ns
t_T	CE Transition Time		20		ns
t_{REF}	Time Between Refresh			2	ms

CAPACITANCE [1]

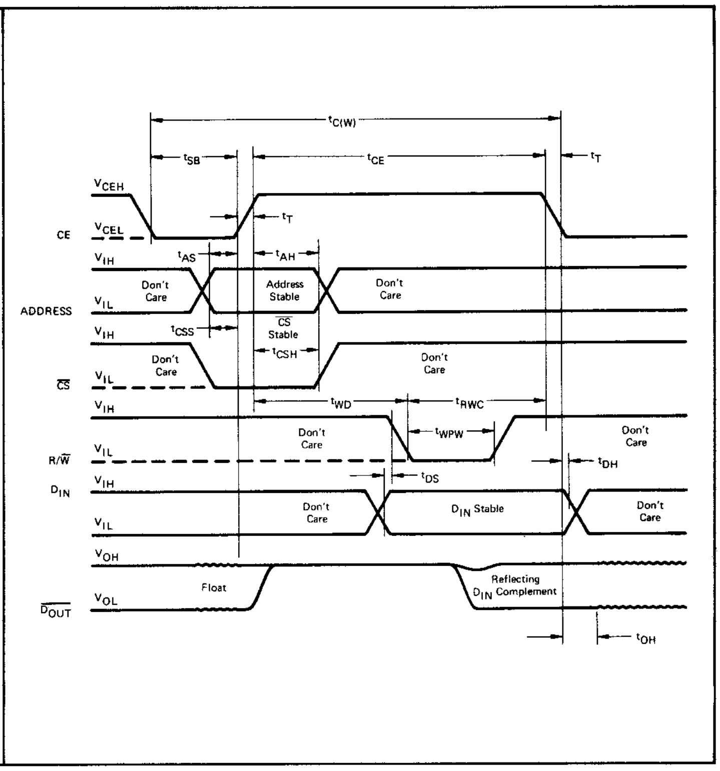
Symbol	Parameter	Typ.	Max.	Unit	Test Conditions [2]
C_{AD}	Address Capacitance, $\overline{CS}$	5	7	pF	$V_{IN} = V_{SS}$
C_{CE}	CE Capacitance	17	25	pF	
C_{IN}	D_{IN} and R/W Capacitance	5	8	pF	
C_{OUT}	D_{OUT} Capacitance	4	6	pF	$V_{OUT} = 0V$

NOTE: [1] All typical values are at $T_A = 25°C$ [2] Capacitance measured with Boonton Meter.

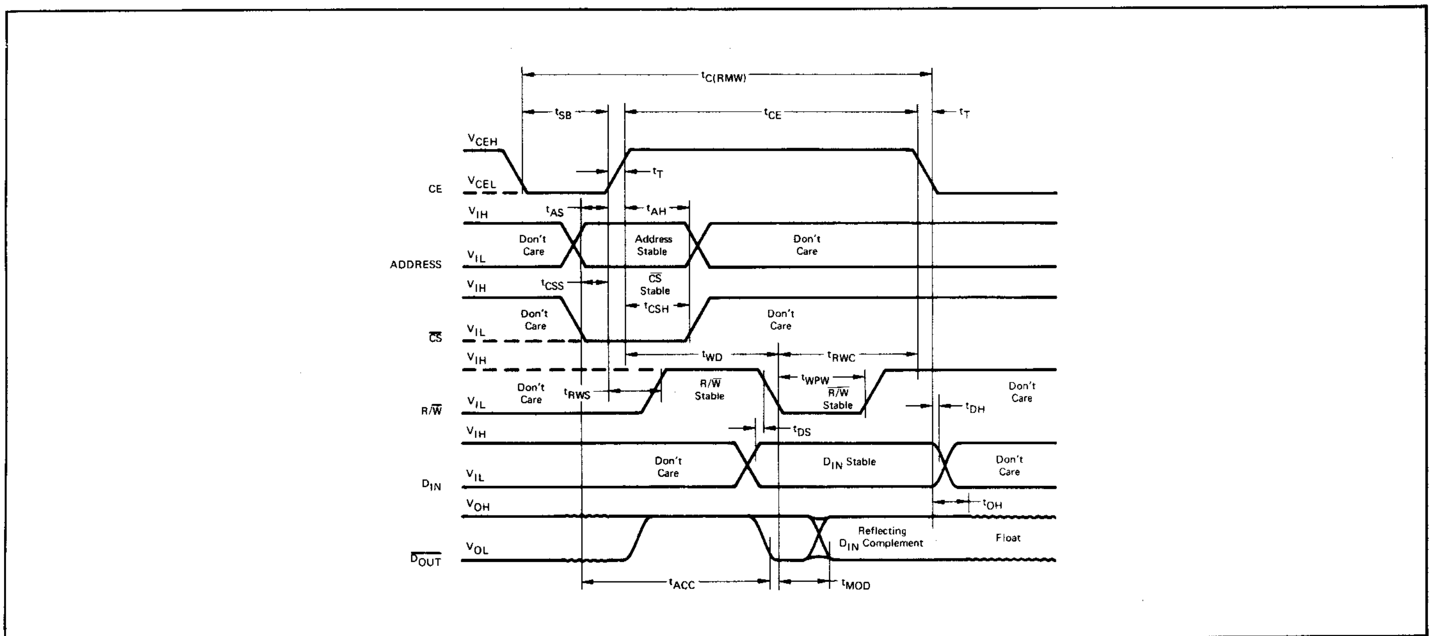
READ AND REFRESH CYCLE



WRITE ONLY CYCLE



READ MODIFY WRITE CYCLE



AMERICAN MICROSYSTEMS, INC.
3800 Homestead Road, Santa Clara, Ca. 95051/Telephone: (408) 246-0330, TWX: 910-338-0018

AMERICAN MICROSYSTEMS, INC.

TERMS OF SALE

1. **ACCEPTANCE:** THE TERMS OF SALE CONTAINED HEREIN APPLY TO ALL QUOTATIONS MADE AND PURCHASE ORDERS ENTERED INTO BY THE SELLER. SOME OF THE TERMS SET OUT HERE MAY DIFFER FROM THOSE IN BUYER'S PURCHASE ORDER AND SOME MAY BE NEW. THIS ACCEPTANCE IS CONDITIONAL ON BUYER'S ASSENT TO THE TERMS SET OUT HERE IN LIEU OF THOSE IN BUYER'S PURCHASE ORDER. SELLER'S FAILURE TO OBJECT TO PROVISIONS CONTAINED IN ANY COMMUNICATION FROM BUYER SHALL NOT BE DEEMED A WAIVER OF THE PROVISIONS OF THIS ACCEPTANCE. ANY CHANGES IN THE TERMS CONTAINED HEREIN MUST SPECIFICALLY BE AGREED TO IN WRITING BY AN OFFICER OF THE SELLER BEFORE BECOMING BINDING ON EITHER THE SELLER OR THE BUYER. All orders or contracts must be approved and accepted by the Seller at its home office. These terms shall be applicable whether or not they are attached to or enclosed with the products to be sold or sold hereunder. Prices for the items described above and acknowledged hereby are firm and not subject to audit, price revision, or price redetermination.

2. **PAYMENT:**
(a) Unless otherwise agreed, all invoices are due and payable thirty (30) days from date of invoice. No discounts are authorized. Shipments, deliveries, and performance of work shall at all times be subject to the approval of the Seller's credit department and the Seller may at any time decline to make any shipments or deliveries or perform any work except upon receipt of payment or upon terms and conditions or security satisfactory to such department.
(b) If, in the judgment of the Seller, the financial condition of the Buyer at any time does not justify continuation of production or shipment on the terms of payment originally specified, the Seller may require full or partial payment in advance and, in the event of the bankruptcy or insolvency of the Buyer or in the event any proceeding is brought by or against the Buyer under the bankruptcy or insolvency laws, the Seller shall be entitled to cancel any order then outstanding and shall receive reimbursement for its cancellation charges.
(c) Each shipment shall be considered a separate and independent transaction, and payment therefor shall be made accordingly. If shipments are delayed by the Buyer, payments shall become due on the date when the Seller is prepared to make shipment. If the work covered by the purchase order is delayed by the Buyer, payments shall be made based on the purchase price and the percentage of completion. Products held for the Buyer shall be at the risk and expense of the Buyer.

3. **TAXES:** Unless otherwise provided herein, the amount of any present or future sales, revenue, excise or other taxes, fees, or other charges of any nature, imposed by any public authority, (national, state, local or other) applicable to the products covered by this order, or the manufacturer or sale thereof, shall be added to the purchase price and shall be paid by the Buyer, or in lieu thereof, the Buyer shall provide the Seller with a tax exemption certificate acceptable to the taxing authority.

4. **F.O.B. POINT:** All sales are made F.O.B. point of shipment. Seller's title passes to Buyer, and Seller's liability as to delivery ceases upon making delivery of material purchased hereunder to carrier at shipping point, the carrier acting as Buyer's agent. All claims for damages must be filed with the carrier. Shipments will normally be made by Parcel Post, Railway Express, Air Express, or Air Freight. Unless specific instructions from Buyer specify which of the foregoing methods of shipment is to be used, the Seller will exercise his own discretion.

5. **DELIVERY:** Shipping dates are approximate and are based upon prompt receipt from Buyer of all necessary information. In no event will Seller be liable for any re-procurement costs, nor for delay or non-delivery, due to causes beyond its reasonable control including, but not limited to, acts of God, acts of civil or military authority, priorities, fires, strikes, lock-outs, slow-downs, shortages, factory or labor conditions, errors in manufacture, and inability due to causes beyond the Seller's reasonable control to obtain necessary labor, materials, or manufacturing facilities. In the event of any such delay, the date of delivery shall, at the request of the Seller, be deferred for a period equal to the time lost by reason of the delay.

In the event Seller's production is curtailed for any of the above reasons so that Seller cannot deliver the full amount released hereunder, Seller may allocate production deliveries among its various customers then under contract for similar goods. The allocation will be made in a commercially fair and reasonable manner. When allocation has been made, Buyer will be notified of the estimated quota made available.

6. **PATENTS:** The Buyer shall hold the Seller harmless against any expense or loss resulting from infringement of patents, trademarks, or unfair competition arising from compliance with Buyer's designs, specifications, or instructions. The sale of products by the Seller does not convey any license, by implication, estoppel, or otherwise, under patent claims covering combinations of said products with other devices or elements.

Except as otherwise provided in the preceding paragraph, the Seller shall defend any suit or proceeding brought against the Buyer, so far as based on a claim that any product, or any part thereof, furnished under this contract constitutes an infringement of any patent of the United States, if notified promptly in writing and given authority, information, and assistance (at the Seller's expense) for defense of same, and the Seller shall pay all damages and costs awarded therein against the Buyer. In case said product, or any part thereof, is, in such suit, held to constitute infringement of patent, and the use of said product is enjoined, the Seller shall, at its own expense, either procure for the Buyer the right to continue using said product or part, replace same with non-infringing product, modify it so it becomes non-infringing, or remove said product and refund the purchase price and the transportation and installation costs thereof. In no event shall Seller's total liability to the Buyer under or as a result of compliance with the provisions of this paragraph exceed the aggregate sum paid by the Buyer for the allegedly infringing product. The foregoing states the entire liability of the Seller for patent infringement by the said products or any part thereof. THIS PROVISION IS STATED IN LIEU OF ANY OTHER EXPRESSED, IMPLIED, OR STATUTORY WARRANTY AGAINST INFRINGEMENT AND SHALL BE THE SOLE AND EXCLUSIVE REMEDY FOR PATENT INFRINGEMENT OF ANY KIND.

7. **INSPECTION:** Unless otherwise specified and agreed upon, the material to be furnished under this order shall be subject to the Seller's standard inspection at the place of manufacture. If it has been agreed upon and specified in this order that Buyer is to inspect or provide for inspection at place of manufacture such inspection shall be so conducted as to not interfere unreasonably with Seller's operations and consequent approval or rejection shall be made before shipment of the material. Notwithstanding the foregoing, if, upon receipt of such material by Buyer, the same shall appear not to conform to the contract, the Buyer shall immediately notify the Seller of such conditions and afford the Seller a reasonable opportunity to inspect the material. No material shall be returned without Seller's consent. Seller's Return Material Authorization form must accompany such returned material.

8. **WARRANTY:** The Seller warrants that the products to be delivered under this purchase order will be free from defects in material and workmanship under normal use and service. Seller's obligations under this Warranty are limited to replacing or repairing or giving credit for, at its option, at its factory, any of said products which shall, within one (1) year after shipment, be returned to the Seller's factory of origin, transportation charges prepaid, and which are, after examination, disclosed to the Seller's satisfaction to be thus defective. THIS WARRANTY IS EXPRESSED IN LIEU OF ALL OTHER WARRANTIES, EXPRESSED, STATUTORY, OR IMPLIED, INCLUDING THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE, AND OF ALL OTHER OBLIGATIONS OR LIABILITIES ON THE SELLER'S PART, AND IT NEITHER ASSUMES NOR AUTHORIZES ANY OTHER PERSON TO ASSUME FOR THE SELLER ANY OTHER LIABILITIES IN CONNECTION WITH THE SALE OF THE SAID ARTICLES. This Warranty shall not apply to any of such products which shall have been repaired or altered, except by the Seller, or which shall have been subjected to misuse, negligence, or accident. The aforementioned provisions do not extend the original warranty period of any product which has either been repaired or replaced by Seller.

It is understood that if this order calls for the delivery of semiconductor devices which are not finished and fully encapsulated, that no warranty, statutory, expressed or implied, including the implied warranty of merchantability and fitness for a particular purpose, shall apply. All such devices are sold as is where is.

9. **GENERAL:**
(a) The validity, performance and construction of these terms and all sales hereunder shall be governed by the laws of the State of California.
(b) The Seller represents that with respect to the production of articles and/or performance of the services covered by this order it will fully comply with all requirements of the Fair Labor Standards Act of 1938, as amended, Williams-Steiger Occupational Safety and Health Act of 1970, Executive Orders 11375 and 11246, Section 202 and 204.
(c) In no event shall Seller be liable for consequential or special damages.
(d) The Buyer may not unilaterally make changes in the drawings, designs or specifications for the items to be furnished hereunder without Seller's prior consent.
(e) Except to the extent provided in Paragraph 10, below, this order is not subject to cancellation or termination for convenience.
(f) Buyer acknowledges that all or part of the products purchased hereunder may be manufactured and/or assembled at any of Seller's facilities, domestic or foreign.
(g) In the event that the cost of the products are increased as a result of increases in materials, labor costs, or duties, Seller may raise the price of the products to cover the cost increases.
(h) If Buyer is in breach of its obligations under this order, Buyer shall remain liable for all unpaid charges and sums due to Seller and will reimburse Seller for all damages suffered or incurred by Seller as a result of Buyer's breach. The remedies provided herein shall be in addition to all other legal means and remedies available to Seller.

10. **GOVERNMENT CONTRACT PROVISIONS:** If Buyer's original purchase order indicates by contract number, that it is placed under a government contract, only the following provisions of the current Armed Services Procurement Regulation are applicable in accordance with the terms thereof, with an appropriate substitution of parties, as the case may be – i.e., "Contracting Officer" shall mean "Buyer", "Contractor" shall mean "Seller", and the term "Contract" shall mean this order:

> 7-103.1, Definitions; 7-103.3, Extras; 7-103.4, Variation in Quantity; 7-103.8, Assignment of Claims; 7-103.9, Additional Bond Security; 7-103.13, Renegotiation; 7-103.15, Rhodesia and Certain Communist Areas; 7-103.16, Contract Work Hours and Safety Standards Act – Overtime Compensation; 7-103.17, Walsh-Healey Public Contracts Act; 7-103.18, Equal Opportunity Clause; 7-103.19, Officials Not to Benefit; 7-103.20, Covenant Against Contingent Fees; 7-103.21, Termination for Convenience of the Government (only to the extent that Buyer's contract is terminated for the convenience of the government); 7-103.22, Authorization and Consent; 7-103.23, Notice and Assistance Regarding Patent Infringement; 7-103.24, Responsibility for Inspection; 7-103.25, Commercial Bills of Lading Covering Shipments Under FOB Origin Contracts; 7-103.27, Listing of Employment Openings; 7-104.4, Notice to the Government of Labor Disputes; 7-104.11, Excess Profit; 7-104.15, Examination of Records by Comptroller General; 7-104.20, Utilization of Labor Surplus Area Concerns.

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